6282 69967

**SEARCH REQUEST FORM** **Scientific and Technical Information Center - EIC2800**

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Date 7/1/02 Serial # 09/849,047 Priority Application Date 5/4/01

Your Name M. Lewis Examiner # ____

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In what format would you like your results? Paper is the default. PAPER DISK EMAIL

**If submitting more than one search, please prioritize in order of need.**

**The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.**

**Where** have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

P12:24

Other: ____

**What** relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. ____

**What** types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other ____

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-13, 17-21, 23-28

Problem: See Page 1 Lines 14-23
" " 2 " 18-29

Solution: " " 3 " 1-30
" " 4 " 1-4

Novelty in structure

Staff Use Only

| Staff Use Only | Type of Search | Vendors |
|---|---|---|
| Searcher: Derrick Blalock | Structure (#) ___ | STN ✓ |
| [redacted] | Bibliographic ✓ | Dialog ___ |
| Searcher Location: STIC-EIC2800, CP4-9C18 | Litigation ___ | Questel/Orbit ___ |
| Date Searcher Picked Up: 7/8/02 | Fulltext ___ | Lexis-Nexis ___ |
| Date Completed: 7-8-02 | Patent Family ___ | WWW/Internet ___ |
| Searcher Prep/Rev Time: 60 | Other ___ | Other ___ |
| Online Time: 60 | | |

?ds

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Set      Items   Description
S1         272   BURIED(3N)(LAYER? OR REGION?)/TI AND (ISOLAT? OR SEPARAT?)-
               /TI
S2          84   S1 AND SUBSTRATE?/TI
S3          65   S2 AND (INTEGRATED()CIRCUIT? OR IC OR ICS OR SEMICONDUCT?)
S4           8   S3 AND (P (3N)TYPE?) AND N(3N)TYPE?
S5           7   S3 AND WELL?
```

t s5/9/2,3,6

**5/9/2 (Item 2 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


014420548 **Image available**
WPI Acc No: 2002-241251/200229
XRPX Acc No: N02-186352
**Analog circuit from** semiconductor substrate isolating **system employs** buried well **and** isolation regions
Patent Assignee: INFINEON TECHNOLOGIES NORTH AMERICA CORP (INFN ); INT BUSINESS MACHINES CORP (IBMC )
Inventor: GUTMANN A; KOTECKI D; KUNKEL G; MANDELMAN J A; PARK Y J
Number of Countries: 021 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200199186 | A2 | 20011227 | WO 2001US19658 | A | 20010620 | 200229 | B |

Priority Applications (No Type Date): US 2000597116 A 20000620
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200199186 | A2 | E | 18 | H01L-023/00 | |

Designated States (National): JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Abstract (Basic): WO 200199186 A2

NOVELTY - **Semiconductor** device has a substrate including mono-crystalline silicon. The substrate includes a P-doped substrate or an N-doped substrate. A buried **well** is formed by patterning a mask over a surface of the substrate, e.g. a resist mask. The buried **well** has a dopant type which is opposite the dopant type of the substrate. A device region is formed near a surface of the substrate and it includes at least one device **well** .

DETAILED DESCRIPTION - A trench region surrounds the device region and extends below the surface of the substrate to at least the buried **well** , so that the device region is isolated from other portions.

USE - In the telecommunications industry.

ADVANTAGE - Noise reduction and improved performance of the circuits.

DESCRIPTION OF DRAWING(S) - The drawing is a cross-sectional view of a **semiconductor** device having a buried **well** .

pp; 18 DwgNo 1/6

Title Terms: ANALOGUE; CIRCUIT; **SEMICONDUCTOR** ; SUBSTRATE; ISOLATE; SYSTEM ; EMPLOY; BURY; **WELL** ; ISOLATE; REGION
Derwent Class: U11; U13
International Patent Class (Main): H01L-023/00
File Segment: EPI
Manual Codes (EPI/S-X): U11-C05B9C; U11-C08A3; U11-D03C3A; U13-B

**5/9/3 (Item 3 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


013724741 **Image available**
WPI Acc No: 2001-208971/200121
XRAM Acc No: C02-056051
XRPX Acc No: N02-137022
**Fabrication of** semiconductor **device on** substrate **involves forming** wells , isolation layers , **gate oxide** layers , buried **contact** regions , **heavily doped regions, gates, and lightly doped drains regions**
Patent Assignee: HYUNDAI MICROSEMICON CO LTD (HYUN-N); HYUNDAI ELECTRONICS IND CO LTD (HYUN-N)
Inventor: PARK S H; PARK S
Number of Countries: 002 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| KR 2000051432 | A | 20000816 | KR 991910 | A | 19990122 | 200121 | B |
| US 6319803 | B1 | 20011120 | US 99373001 | A | 19990812 | 200224 | |
| KR 275965 | B | 20001215 | KR 991910 | A | 19990122 | 200175 | |

Priority Applications (No Type Date): KR 991910 A 19990122

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| KR 2000051432 | A | | | H01L-021/336 | |
| US 6319803 | B1 | | 10 | H01L-021/44 | |
| KR 275965 | B | | | H01L-021/336 | Previous Publ. patent KR 2000051432 |

Abstract (Basic): US 6319803 B1

NOVELTY - A **semiconductor** device is fabricated on a substrate (111) by forming **wells** in the substrate; forming isolation layers (113) in the substrate; forming gate oxide layers on the first and second **wells** ; forming buried contact regions in the substrate; forming heavily doped regions in the buried contact regions; forming gates on the first **well** ; and forming lightly doped drains regions.

DETAILED DESCRIPTION - Fabrication of **semiconductor** device on a substrate involves

(i) forming first and second **wells** (121, 122) in the substrate;

(ii) forming first, second, and third isolation layers in the substrate;

(iii) forming first and second gate oxide layers on the first and second **wells** ;

(iv) forming first and second buried contact regions in the substrate;

(v) forming first and second heavily doped regions (145, 147) in the first and second buried contact regions;

(vi) forming first and third gates (137a-d) on the first **well** , the second and fourth gates on the second **well** , the third and fourth gates directly contacting the second and first buried contact regions, respectively;

(vii) forming a pair of lightly doped drain (LDD) regions (140) at both sides of the first gate as a mask; and

(viii) forming second pair of LDD regions at both sides of the second gate using the second gate as a mask. One of LDD regions is positioned between the second gate and the first buried contact region.

USE - For fabricating a **semiconductor** device on a substrate.

ADVANTAGE - The invented method provides a simplified process that increases a yield in fabricating **semiconductor** devices.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view illustrating the fabrication of a **semiconductor** device.

Substrate (111)

Isolation layers (113)

**Wells** (121, 122)

Gates (137a-d)

LDD regions (140)

Heavily doped regions (145, 147)

pp; 10 DwgNo 2D/2

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The method further comprises forming spacers on both sides of the gates; forming first and second pairs of heavily doped regions at both sides of the first and third gates using the gates including spacers as masks; and forming a planarization layer on the substrate including the gates. The first buried contact region is formed between the second and fourth gate, and the second buried contact region is formed between the first and third gate. The first gate is formed on the first gate oxide layer, and the second gate is formed on the second gate oxide layer. The step of forming first and second heavily doped regions includes ion implantation of second and first type conductivity ions, respectively with a dose of 1x1015-5x1015, preferably 1x1015-3x1015 atoms/cm2 at an acceleration energy of 30 KeV and at annealing temperature of 900-1000degreesC. The step of forming first and second pairs of lightly

doped drain regions includes the step of implanting second and first type conductivity ions, respectively with a dose of 1x1013-1x1014 atoms/cm2.
Title Terms: FABRICATE; **SEMICONDUCTOR** ; DEVICE; SUBSTRATE; FORMING; **WELL** ; ISOLATE; LAYER; GATE; OXIDE; LAYER; BURY; CONTACT; REGION; HEAVY; DOPE; REGION; GATE; LIGHT; DOPE; DRAIN; REGION
Derwent Class: L03; U11; U13
International Patent Class (Main): H01L-021/336; H01L-021/44
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C02B; L04-C13B
Manual Codes (EPI/S-X): U11-C18A3; U13-D02A

**5/9/6 (Item 6 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


009823410 **Image available**
WPI Acc No: 1994-103266/199413
Related WPI Acc No: 1996-202296; 2002-207696; 2002-207697; 2002-207698; 2002-228915; 2002-228916
XRPX Acc No: N94-080633
Isolated well **structure for transistor in BiCDMOS** integrated circuit **process - has vertical transistor formed in** well **at upper surface of epitaxial layer,** separated **and** isolated **from** substrate layer **by** buried well **in epilayer and** buried isolation region **in epilayer and** substrate
Patent Assignee: SILICONIX INC (SILI-N)
Inventor: CHEN J W; CORNELL M E; WILLIAMS R K; YILMAZ H; CHEN W
Number of Countries: 006 Number of Patents: 008
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 589675 | A2 | 19940330 | EP 93307457 | A | 19930921 | 199413 | B |
| US 5374569 | A | 19941220 | US 92948276 | A | 19920921 | 199505 | |
| | | | US 9326932 | A | 19930305 | | |
| JP 7007094 | A | 19950110 | JP 93254786 | A | 19930917 | 199511 | |
| US 5416039 | A | 19950516 | US 92948276 | A | 19920921 | 199525 | |
| | | | US 9326713 | A | 19930305 | | |
| | | | US 94225270 | A | 19940408 | | |
| US 5422508 | A | 19950606 | US 92948276 | A | 19920921 | 199528 | |
| | | | US 9326930 | A | 19930305 | | |
| US 5426328 | A | 19950620 | US 92948276 | A | 19920921 | 199530 | |
| | | | US 94226419 | A | 19940411 | | |
| EP 589675 | A3 | 19941117 | EP 93307457 | A | 19930921 | 199536 | |
| US 5751054 | A | 19980512 | US 92948276 | A | 19920921 | 199826 | |
| | | | US 9326932 | A | 19930305 | | |
| | | | US 94335526 | A | 19941107 | | |
| | | | US 96705910 | A | 19960829 | | |

Priority Applications (No Type Date): US 92948276 A 19920921; US 9326932 A 19930305; US 9326713 A 19930305; US 94225270 A 19940408; US 9326930 A 19930305; US 94226419 A 19940411; US 94335526 A 19941107; US 96705910 A 19960829
Cited Patents: No-SR.Pub; GB 2253091; US 4855244
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 589675 | A2 | E | 64 | H01L-027/06 | |
| Designated States (Regional): DE FR IT NL | | | | | |
| US 5374569 | A | | 56 | H01L-021/265 | Div ex application US 92948276 |
| JP 7007094 | A | | 39 | H01L-021/8249 | |
| US 5416039 | A | | 57 | H01L-021/266 | Div ex application US 92948276 |
| | | | | | Cont of application US 9326713 |
| US 5422508 | A | | 56 | H01L-029/784 | Div ex application US 92948276 |
| US 5426328 | A | | 37 | H01L-029/70 | Cont of application US 92948276 |
| EP 589675 | A3 | | | H01L-027/06 | |
| US 5751054 | A | | | H01L-029/861 | Div ex application US 92948276 |
| | | | | | Cont of application US 9326932 |

Cont of application US 94335526
Cont of patent US 5374569

Abstract (Basic): EP 589675 A

The isolated **well** structure includes an epitaxial layer on a **semiconductor** substrate layer of opposite conductivity. A buried isolation region extends into the substrate and epitaxial layers, beneath the epilayer upper surface and is of the same conductivity type as the substrate. A buried **well** in the epitaxial layer, and of the same conductivity type, extends upward from the buried isolation region upper surface.

A **well** region in the epitaxial layer, of the same conductivity, extends down from the upper surface of the layer. The **well** region lower surface contacts the top of the buried **well** . The **well** and buried **well** are both electrically isolated and separated from the substrate. The **well** region is of the first conductivity type. A transistor is formed in the **well** at the upper surface of the epitaxial layer.

USE/ADVANTAGE - Complementary bipolar transistor analog circuitry, CMOS transistors for high power digital switching and digital logic circuitry, DMOS power transistors, buried Zener diodes, thin film resistors, all in single wafer or **IC** . Fewer masking steps in mfr.; improved yield.

Dwg.18/26

Abstract (Equivalent): US 5426328 A

The method involves using an isolation structure to isolate an MOS transistor from a bipolar transistor. The isolation structure comprises a buried isolation region extending downward into a substrate layer of a **semiconductor** material of a first conductivity type, and also extending upward into an epitaxial layer of a **semiconductor** material of a second conductivity type. The epitaxial layer having a thickness of at least approximately eight microns, is disposed over the substrate layer. The buried isolation region of a **semiconductor** material of the second conductivity type, has an upper surface disposed below an upper surface of the epitaxial layer.

A buried **well** region of first conductivity type is disposed only in the epitaxial layer, and extends upward from the upper surface of the buried isolation layer so that the buried **well** region is separated and electrically isolated from the substrate layer. A **well** region is disposed in the epitaxial layer. A lower surface of the **well** region contacts the upper surface of the buried **well** region so that the **well** region is separated and electrically isolated from the substrate layer. The bipolar transistor is formed in the **well** region at the upper surface of the epitaxial layer, and the MOS transistor is formed at the upper surface of the epitaxial layer but outside the **well** region.

USE/ADVANTAGE - Can be used to produce CMOS transistors, DMOS power transistors, buried Zener diodes and associated structures simultaneously on single wafer, for use in high power digital switching, analog amplification and digital logic circuitry for use in telecommunications, automotive, and computer industries.

Dwg.19/26

US 5422508 A

A body region extends from a body contact region and underneath a source region. The body region extends between the source region and a field implant region to form a channel region at the upper surface of a second **semiconductor** layer between the source region and the field implant region. The body region is separated from the field implant region by a drift region portion of the second layer, with the body contact region being of the same **semiconductor** material.

A polysilicon gate layer extends from a location over the source region, over the channel region, and over the drift region portion of the second layer.

ADVANTAGE - Simultaneously forms high quality complementary bipolar transistors, relatively high voltage CMOS transistors, relatively low voltage CMOS transistors, DMOS transistors, zener diodes and thin-film resistors, or any desired combination of these, all on the same

**integrated circuit** chip. The process uses a small number of masking steps, forms high performance transistor structures, and results in a high yield of functioning die.

Dwg.24/26

US 5416039 A

The isolation structure formation on a **semiconductor** material substrate involves doping an area on an upper surface of the substrate opposite the substrate conductivity, and doping a second area, within the initial area, the same as the substrate conductivity. An epitaxial layer is formed over the substrate upper surface of opposite conductivity, with a thickness of at least about 8mum and having a doping concn. within about 5E15 to 2E16 atoms/cm3.

A **well** is extended into the epilayer from the upper surface, positioned at least partly over the second doped area in the substrate. The **well** region has a bottom surface which contacts a buried **well** region formed by the dopants of the first conductivity type which doped the second area in the substrate.

USE/ADVANTAGE - Integrates complementary bipolar transistors, high voltage CMOS transistors, low voltage CMOS transistors, DMOS transistors, zener diodes and thin-film resistors, with isolation structures. Small number of masking steps, high yield of functioning die.

Dwg.16D/26

US 5374569 A

The single wafer used comprises an epitaxial layer having an upper surface, the epitaxial layer being doped with a dopant of a first conductivity type. A MOS transistor is formed in a MOS region of the wafer. Buried Zener diodes are formed in a Zener region of the wafer.

The method comprises the steps of: forming a set of laterally separated first Zener portions in the upper surface of the epitaxial layer in the Zener region, each of these portions being doped with a dopant of a second conductivity type opposite the first conductivity type. A light ion implantation step uses a dopant of the first conductivity type to form simultaneously a source and a drain in the MOS region and to form simultaneously at least one second Zener portion in the Zener region.

ADVANTAGE - Uses small number of masking steps, forms high performance transistor structures and results in high yield of functioning die.

Dwg.17/26

Title Terms: ISOLATE; **WELL** ; STRUCTURE; TRANSISTOR; INTEGRATE; CIRCUIT; PROCESS; VERTICAL; TRANSISTOR; FORMING; **WELL** ; UPPER; SURFACE; EPITAXIAL ; LAYER; SEPARATE; ISOLATE; SUBSTRATE; LAYER; BURY; **WELL** ; EPILAYER; BURY; ISOLATE; REGION; EPILAYER; SUBSTRATE

Derwent Class: U11; U12; U13

International Patent Class (Main): H01L-021/265; H01L-021/266; H01L-021/8249; H01L-027/06; H01L-029/70; H01L-029/784; H01L-029/861

International Patent Class (Additional): H01L-021/82; H01L-023/62; H01L-027/102; H01L-029/73; H01L-029/76; H01L-029/94

File Segment: EPI

Manual Codes (EPI/S-X): U11-C08A1; U12-D01A9; U12-D02A9; U12-Q; U13-D03B1; U13-D03B2

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?t s4/9/1,2,3,4,5,6,8

**4/9/1 (Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


010457472 **Image available**
WPI Acc No: 1995-358791/199546
XRPX Acc No: N95-266604

**Low voltage CMOS transistor for high voltage charge pump circuit - includes** buried N - type isolation layer **underlying source, drain and gate electrode which sustains voltage impressed on source region differing more than five volts from voltage impressed on** substrate

Patent Assignee: NAT SEMICONDUCTOR CORP (NASC )
Inventor: MERRILL R B; YOUNG W
Number of Countries: 018 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 9527310 | A1 | 19951012 | WO 95US3782 | A | 19950324 | 199546 | B |
| US 5475335 | A | 19951212 | US 94221602 | A | 19940401 | 199604 | |
| | | | US 94319902 | A | 19941007 | | |
| EP 701737 | A1 | 19960320 | EP 95914892 | A | 19950324 | 199616 | |
| | | | WO 95US3782 | A | 19950324 | | |
| US 5622885 | A | 19970422 | US 94221602 | A | 19940401 | 199722 | |
| | | | US 95483214 | A | 19950607 | | |
| US 5786617 | A | 19980728 | US 94221602 | A | 19940401 | 199837 | |
| | | | US 95556295 | A | 19951005 | | |
| EP 921627 | A2 | 19990609 | EP 95914892 | A | 19950324 | 199927 | |
| | | | EP 99100290 | A | 19950324 | | |

Priority Applications (No Type Date): US 94221602 A 19940401; US 94319902 A 19941007; US 95483214 A 19950607; US 95556295 A 19951005
Cited Patents: 1.Jnl.Ref; EP 450797; JP 5190783; JP 62073755; US 4825275; US 5323043
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 9527310 | A1 | | 35 | H01L-027/02 | |
| Designated States (National): DE KR | | | | | |
| Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE | | | | | |
| US 5475335 | A | | 15 | G05F-001/10 | Div ex application US 94221602 |
| EP 701737 | A1 | E | 35 | H01L-027/02 | Based on patent WO 9527310 |
| Designated States (Regional): DE FR GB | | | | | |
| US 5622885 | A | | 15 | H01L-021/761 | Div ex application US 94221602 |
| US 5786617 | A | | | H01L-027/092 | Cont of application US 94221602 |
| EP 921627 | A2 | E | | H02M-003/07 | Div ex application EP 95914892 |
| | | | | | Div ex patent EP 701737 |
| Designated States (Regional): DE GB | | | | | |

Abstract (Basic): WO 9527310 A

The transistor comprises a substrate with a principal surface doped to a **P - type** conductivity with **N - type** source and drain regions spaced apart and extending to the principal surface. A gate electrode overlies the principal surface between the source and drain regions.

An **N - type** isolation layer is formed in the **integrated circuit** substrate, underlying the source and the drain and gate electrode and is spaced apart from the source and drain regions and from the backside surface of the substrate. The transistor sustains a voltage impressed on the source region differing by more than 5 volts from a voltage impressed on the substrate.

ADVANTAGE - Combines high density low voltage standard CMOS logic transistors with CMOS transistors operating at high voltage on same chip.

Dwg.9/11

Abstract (Equivalent): US 5622885 A

A method of forming a plurality of transistors in a substrate, the transistors being capable of operating at a range of voltages relative to one another, comprising the steps of:

providing a substrate having a principal surface and doped to have a first conductivity type;

forming a plurality of spaced-apart isolation regions in the substrate, each isolation region doped to have a second conductivity type;

forming over each isolation region and extending from the isolation region to the principal surface a first well of the first conductivity type and a second well of the second conductivity type;

forming a source and a drain region spaced apart in each of the wells of the first conductivity type, each source and drain region extending to the principal surface layer and doped to have the second conductivity type;

forming a source and a drain region spaced apart in each of the wells of the second conductivity type, each source and drain region extending to the principal surface and doped to have the first conductivity type;

forming a plurality of gate electrodes overlying the principal surface of the substrate, each gate electrode lying between one of the source and drain regions;

forming in each well a well contact region doped to have the same conductivity type as the well and being more highly doped than the well and extending to the principal surface; and

connecting each of the well contact regions to a different voltage level;

wherein a first of the transistors is electrically isolated from the second of the transistors and from the substrate by the isolation regions.

Dwg.2/9

US 5475335 A

We claim:

1. A cascaded charge pump circuit formed on a single **semiconductor** substrate, comprising:

a plurality of N charge pumps, each charge pump i having a first and second input terminal and an output terminal;

a voltage supply terminal;

a voltage reference terminal;

and a circuit output terminal;

wherein the first input terminal of a first charge pump i=1 in the plurality of charge pumps is connected to the voltage supply terminal, and the second input terminal of the first charge pump is connected to the voltage reference terminal;

and wherein for each successive charge pump i, where i=2 to N, in the plurality of charge pumps, the first input terminal is connected to the output terminal of the i-1 charge pump, and the second input terminal is connected to the first input terminal of the i-1 charge pump;

and wherein the output terminal of the charge pump i=N is connected to the circuit output terminal; and

each charge pump is electrically isolated on the **semiconductor** substrate from the other charge pumps.

Dwg.5a/9

Title Terms: LOW; VOLTAGE; CMOS; TRANSISTOR; HIGH; VOLTAGE; CHARGE; PUMP; CIRCUIT; BURY; N; TYPE; ISOLATE; LAYER; UNDERLYING; SOURCE; DRAIN; GATE; ELECTRODE; SUSTAINED; VOLTAGE; IMPRESS; SOURCE; REGION; DIFFER; MORE; FIVE; VOLT; VOLTAGE; IMPRESS; SUBSTRATE

Derwent Class: U11; U13; U24

International Patent Class (Main): G05F-001/10; H01L-021/761; H01L-027/02; H01L-027/092; H02M-003/07

International Patent Class (Additional): G05F-003/02

File Segment: EPI

Manual Codes (EPI/S-X): U11-C08A1; U13-D02A; U24-D02A

**4/9/2 (Item 2 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

009708683
WPI Acc No: 1993-402236/199350
**Integrated injection logic** semiconductor **device with improved operation speed and reduced power consumption - includes P** substrate **with N+** buried layer **, N epilayer and P+** isolation **regions, and has** n - type **active regions within** p - type **active regions adjacent field oxide films NoAbstract**
Patent Assignee: SAMSUNG ELECTRONICS CO (SMSU )
Inventor: KANG H; KIM H
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| KR 9304299 | B | 19930522 | KR 9019299 | A | 19901128 | 199350 | B |

Priority Applications (No Type Date): KR 9019299 A 19901128
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| KR 9304299 | B | | | H01L-027/08 | |

Title Terms: INTEGRATE; INJECTION; LOGIC; **SEMICONDUCTOR** ; DEVICE; IMPROVE; OPERATE; SPEED; REDUCE; POWER; CONSUME; P; SUBSTRATE; N; BURY; LAYER; N; EPILAYER; P; ISOLATE; REGION; **N - TYPE** ; ACTIVE; REGION; **P - TYPE** ; ACTIVE; REGION; ADJACENT; FIELD; OXIDE; FILM; NOABSTRACT
Derwent Class: U13; U21
International Patent Class (Main): H01L-027/08
File Segment: EPI

**4/9/3 (Item 3 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


008781684 **Image available**
WPI Acc No: 1991-285701/199139
XRPX Acc No: N91-218563
**Bipolar** IC **device - has** p - type isolation **regions formed in** n - type **epitaxial** layer **on p-** type buried layer **of** substrate **NoAbstract Dwg 1/2**
Patent Assignee: MATSUSHITA ELECTRONICS CORP (MATE )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 3190261 | A | 19910820 | JP 89330589 | A | 19891220 | 199139 | B |

Priority Applications (No Type Date): JP 89330589 A 19891220
Title Terms: BIPOLAR; **IC** ; DEVICE; **P - TYPE** ; ISOLATE; REGION; FORMING; **N - TYPE** ; EPITAXIAL; LAYER; **P - TYPE** ; BURY; LAYER; SUBSTRATE; NOABSTRACT
Derwent Class: U11; U12
International Patent Class (Additional): H01L-021/76; H01L-029/73
File Segment: EPI
Manual Codes (EPI/S-X): U11-C02J5; U11-C08A1; U12-D01A

**4/9/4 (Item 4 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


008318779 **Image available**
WPI Acc No: 1990-205780/199027
Semiconductor IC **device mfr. with MIS capacitor element - by forming** N - type buried regions **in** P - type isolation **region in surface of** P - type substrate **, depositing epitaxial layer NoAbstract Dwg 1/2**
Patent Assignee: SANYO ELECTRIC CO (SAOL )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 2137258 | A | 19900525 | JP 88291453 | A | 19881117 | 199027 | B |

Priority Applications (No Type Date): JP 88291453 A 19881117
Title Terms: **SEMICONDUCTOR** ; **IC** ; DEVICE; MANUFACTURE; MIS; CAPACITOR; ELEMENT; FORMING; N; TYPE; BURY; REGION; P; TYPE; ISOLATE; REGION; SURFACE; P; TYPE; SUBSTRATE; DEPOSIT; EPITAXIAL; LAYER; NOABSTRACT
Derwent Class: L03; U11; U12; U13
International Patent Class (Additional): H01L-027/04
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C02D; L04-C10G; L04-C11C
Manual Codes (EPI/S-X): U11-C05G1; U12-C02A; U13-D01

**4/9/5 (Item 5 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


008254009 **Image available**
WPI Acc No: 1990-141010/199019
XRPX Acc No: N90-109356
Buried **-doped-** region integrated circuit **formation - using higher than normal doping level in** substrate **to provide sufficient boron for** isolation
Patent Assignee: TEXAS INSTR INC (TEXI )
Inventor: BELL D A; HAVEMANN R H
Number of Countries: 007 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| EP 366967 | A | 19900509 | EP 89118454 | A | 19891005 | 199019 | B |
| JP 2244737 | A | 19900928 | | | | 199045 | |
| US 5310690 | A | 19940510 | US 88265074 | A | 19881031 | 199418 | |
| | | | US 90632437 | A | 19901221 | | |
| | | | US 92880477 | A | 19920506 | | |
| US 5451530 | A | 19950919 | US 90632437 | A | 19901221 | 199543 | N |
| | | | US 92880477 | A | 19920506 | | |
| | | | US 94179849 | A | 19940111 | | |
| EP 366967 | B1 | 19970521 | EP 89118454 | A | 19891005 | 199725 | |
| DE 68928060 | E | 19970626 | DE 628060 | A | 19891005 | 199731 | |
| | | | EP 89118454 | A | 19891005 | | |

Priority Applications (No Type Date): US 88265074 A 19881031; US 90632437 A 19901221; US 92880477 A 19920506; US 94179849 A 19940111
Cited Patents: A3...9139; EP 253724; EP 278619; EP 67661; EP 97379; NoSR.Pub
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 366967 | A | | | | |
| Designated States (Regional): DE FR GB IT NL | | | | | |
| US 5310690 | A | | 9 | H01L-021/265 | Cont of application US 88265074 |
| | | | | | Cont of application US 90632437 |
| US 5451530 | A | | | H01L-021/761 | Cont of application US 90632437 |
| | | | | | Cont of application US 92880477 |
| | | | | | Cont of patent US 5310690 |
| EP 366967 | B1 | E | 11 | H01L-021/82 | |
| Designated States (Regional): DE FR GB IT NL | | | | | |
| DE 68928060 | E | | | H01L-021/82 | Based on patent EP 366967 |

Abstract (Basic): EP 366967 A
A thermal oxide layer (26) is formed over a portion of a **p - type** substrate (20) at which an n+ buried doped region (30) is not to be formed, masking the implant for the buried doped region (30). Anneal of the implant is performed in an oxidising atmosphere, growing further oxide (28) over the surface. The oxide layers (26,28) are removed, and a **p - type** blanket implant is performed for isolation purposes and, if desired, to form a **p - type** buried doped region (31). The doping concentration of the n+ buried doped region (30) retards diffusion of the boron to the surface.

Alternately, a higher than normal doping level in the substrate

can provide sufficient boron for isolation. An epitaxial layer (32) is then grown over the surface, and the n-well (40) is formed by implanting **n - type** dopant, with the **p** -well regions masked by a nitride mask; anneal of the n-well is also done in an oxidising environment, so that consumption of a portion of the n-well (40) by the oxide (42) further planarises the topography of the device.

USE/ADVANTAGE - Subcollectors in bipolar **ic** BiCMOS. Reduced defect density after annealing.

Dwg.3h/4

Abstract (Equivalent): EP 366967 B

A method of fabricating an **integrated circuit** at a surface of a **semiconductor** (20) of a first conductivity type, comprising

forming a first oxide layer (26) at a first location of the surface, doping a second location (30) of the surface not masked by the first oxide layer, by implanting a dopant of a second conductivity type, annealing the **semiconductor** in an oxidizing ambient thereby diffusing said dopant into the second location and thereby thickening said first oxide layer and forming a second oxide layer (28) on the surface at the second location, implanting both said first and said second location with dopant of the first conductivity type through said first and second oxide layers, removing the oxide layers,

forming an epitaxial layer over said first and second locations after said implanting step, so that said doped second location of the surface forms a buried doped region.

Dwg.3a/4

Abstract (Equivalent): US 5310690 A

The method involves forming a thermal oxide layer over a portion of a **p - type** substrate at which an n+ buried doped region is not to be formed, masking the implant for the buried doped region. Anneal of the implant is performed in an oxidizing atmosphere, growing further oxide over the surface. The oxide layers are removed, and a **p - type** blanket implant is performed for isolation purposes and, if desired, to form a **p - type** buried doped region; the doping concentration of the n+ buried doped region retards diffusion of the boron to the surface.

Alternatively, a higher than normal doping level in the substrate can provide sufficient boron for isolation. An epitaxial layer is then grown over the surface, and the n-well is formed by implanting **n - type** dopant, with the **p** -well regions masked by a nitride mask; anneal of the n-well is also done in an oxidizing environment, so that consumption of a portion of the n-well by the oxide further planarises the topography of the device.

ADVANTAGE - Results in improved planar topography. Has reduced defect density after annealing steps.

Dwg.3i/4

Title Terms: BURY; DOPE; REGION; INTEGRATE; CIRCUIT; FORMATION; HIGH; NORMAL; DOPE; LEVEL; SUBSTRATE; SUFFICIENT; BORON; ISOLATE

Derwent Class: U11; U12; U13

International Patent Class (Main): H01L-021/265; H01L-021/761; H01L-021/82

International Patent Class (Additional): H01L-021/74

File Segment: EPI

Manual Codes (EPI/S-X): U11-C02J5; U11-C08A2; U11-C08A5; U12-D01A; U13-D02A ; U13-D03

**4/9/6 (Item 6 from file: 350)**

DIALOG(R)File 350:Derwent WPIX



003146160

WPI Acc No: 1981-06702D/198105

**Forming insulation** isolation **regions in** semiconductor substrate - **by forming aluminium ion implanted regions in** P - type **silicon** substrate **, forming** N **(plus)-** type buried **collector** region **etc.**

Patent Assignee: MATSUSHITA ELECTRONICS CORP (MATE )

Number of Countries: 002 Number of Patents: 003

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| JP 55151349 | A | 19801125 | JP 7960131 | A | 19790515 | 198105 | B |
| US 4295898 | A | 19811020 | | | | 198145 | |
| JP 88061777 | B | 19881130 | | | | 198851 | |

Priority Applications (No Type Date): JP 7960131 A 19790515

Abstract (Basic): JP 55151349 A

Al ion-implanted regions are formed in a **p - type** Si substrate. An **n** (+)- **type** buried collector region is formed in the substrate by diffusion of As. An **n - type** epitaxial layer is formed on the substrate. A SiO2 film is formed on the epitaxial layer and windows for ion implantation are made in the SiO2 film. Al ions and B ions are implanted into the epitaxial layer through the windows to form ion implanted regions.

The substrate is annealed to activate Al and B, and then heated at 1200 deg.C for 3 hrs. to perform drive-in diffusion. Al atoms in the **p** (+)- **type** region and the ion-implanted regions are diffused into the epitaxial layer by heat treatment to form **p** (+)- **type** regions, which are united as one body to form insulating isolation regions. Island regions are formed in the substrate.

Title Terms: FORMING; INSULATE; ISOLATE; REGION; **SEMICONDUCTOR** ; SUBSTRATE ; FORMING; ALUMINIUM; ION; IMPLANT; REGION; **P - TYPE** ; SILICON; SUBSTRATE; FORMING; N; PLUS; TYPE; BURY; COLLECT; REGION
Derwent Class: L03; U11
International Patent Class (Additional): H01L-021/76
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-D03A; L03-D03D

**4/9/8 (Item 8 from file: 350)**
DIALOG(R)File 350:Derwent WPIX


002227395
WPI Acc No: 1979-26575B/197914

**Dielectric** isolation **type** semiconductor integrated circuit substrate **- prepd. on** p - type **silicon** substrate **with** buried **n-plus** regions

Patent Assignee: NIPPON ELECTRIC CO (NIDE )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 54006783 | A | 19790119 | | | | 197914 | B |

Priority Applications (No Type Date): JP 7772455 A 19770617

Abstract (Basic): JP 54006783 A

Substrate comprises a **p - type** silicon substrate with **n** + buried regions on it; **n - type** islands disposed on the **p - type** silicon substrate, electrically isolated from each other by a dielectric isolation region disposed between the islands; and n+ regions formed around each island so as to connect to each n+ buried region.

The structure is made by (a) prepg. a **p - type** Si substrate with **n** + buried regions; (b) forming a silicon oxide film pattern between the n+ regions; (c) epitaxially forming an **n - type** layer and a polycrystalline silicon region on the pattern; (d) diffusing an **n - type** impurity into the polycrystalline region; (e) converting the region into a porous silicon region by anodic treatment; (f) diffusing the **n - type** impurity from the porous silicon region into the **n - type** island; and (g) oxidising the porous silicon region to form the dielectric isolation region.

The n+ region serves as a collector contact region which reduces the collector series resistance. The substrate is obtd. easily and quickly

Title Terms: DIELECTRIC; ISOLATE; TYPE; **SEMICONDUCTOR** ; INTEGRATE; CIRCUIT ; SUBSTRATE; PREPARATION; **P - TYPE** ; SILICON; SUBSTRATE; BURY; N; PLUS; REGION

Index Terms/Additional Words: **N-TYPE**
Derwent Class: L03; U11; U12; U13
International Patent Class (Additional): H01L-021/76; H01L-027/04
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-D03; L03-D04; L03-H02
?

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     FILE 'WPIX, JAPIO' ENTERED AT 12:43:53 ON 08 JUL 2002
L1       683704 S IC OR ICS OR INTEGRATED(W)CIRCUIT OR (MICRO)(W)(CIRCUIT OR CH
L2       307609 S TRANSISTOR
L3        30349 S CONDUCT?(W)TYPE
L4         4303 S ((WELL)(W)(REGION OR AREA OR ZONE))
L5         6200 S ((BURIED)(W)(LAYER OR FILM OR COAT####))
L6         8968 S (DOPED OR DOPING)(2N)(REGION OR ZONE OR AREA)
L7          245 S CONTACT(W)DIFFUSION
L8        66647 S ION(W)IMPLANT######
L9        19327 S ((EPITAXIAL)(W)(LAYER OR FILM OR COAT####))
L10          68 S L1 AND L7
L11          28 S L10 AND L2
L12       51952 S L1 AND L2
L13        2525 S L12 AND L3
L14         163 S L13 AND L4
L15          27 S L14 AND L6
L16          27 S L15 NOT L11
L17          78 S L2 AND L7
L18           6 S L17 AND L4
L19           4 S L18 NOT (L11 OR L15)
L20         324 S L13 AND L8
L21          73 S L20 AND L9
L22          70 S L21 NOT (L11 OR L16 OR L18)
L23           4 S L22 AND L6
L24          27 S L22 AND L5

     FILE 'DPCI' ENTERED AT 13:07:42 ON 08 JUL 2002
L25          30 S (US4814288 OR US4862242 OR 4881107)/PN.D,PN.G
L26         107 S (US4881107 OR US4912054 OR US4921811 OR US5014106 OR US514825
L27          91 S (US5438009 OR US5536962 OR US5623159 OR US5691224 OR US569122

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     FILE 'DPCI' ENTERED AT 13:13:19 ON 08 JUL 2002
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L28         SEL L25 1- PN :      183 TERMS
                SET SMARTSELECT OFF

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L29          43 S L28

     FILE 'DPCI' ENTERED AT 13:13:38 ON 08 JUL 2002
                SET SMARTSELECT ON
L30         SEL L26 1- PN :      428 TERMS
                SET SMARTSELECT OFF

     FILE 'WPIX, JAPIO' ENTERED AT 13:13:50 ON 08 JUL 2002
L31         184 S L30

     FILE 'DPCI' ENTERED AT 13:14:10 ON 08 JUL 2002
                SET SMARTSELECT ON
L32         SEL L27 1- PN :      204 TERMS
                SET SMARTSELECT OFF

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L33         127 S L32
L34         346 S L29 OR L31 OR L33
L35          89 S L11 OR L15 OR L18 OR L23 OR L24
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| | | |
|---|---|---|
| L36 | 344 | S L34 NOT L35 |
| L37 | 148 | S L36 AND L1 |
| L38 | 85 | S L37 AND L2 |
| L39 | 27 | S L38 AND L3 |
| L40 | 6 | S L38 AND L4 |
| L41 | 30 | S L39 OR L40 |

L11 ANSWER 1 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 2001-637643 [73] WPIX
CR 1999-508296 [42]
DNN N2001-476477
TI Integrated circuitry for N-metal oxide semiconductor **transistor**, has well **contact diffusion** regions formed in well extension region of rectangular shape.
DC U13
IN BATRA, S; KERR, R; TRAN, L C; WU, Z; YANG, R
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6215151 B1 20010410 (200173)* 14p
ADT US 6215151 B1 Div ex US 1997-912108 19970804, US 1999-255667 19990223
FDT US 6215151 B1 Div ex US 5946564
PRAI US 1997-912108 19970804; US 1999-255667 19990223
AB US 6215151 B UPAB: 20011211
NOVELTY - A p-type well region (16) is formed on a substrate (12). A extension well region (14) is formed extending away from well region. A p-type well **contact diffusion** region (38) is formed within the extension well region, which contains with well region. The extension well region has rectangular shape.

USE - For N- and P type metal oxide semiconductor (NMOS, PMOS) **transistors**, Complementary metal oxide semiconductor **transistor** (
u13-d2a
CMOS).

ADVANTAGE - Suitably dimensional single mask opening is provided and unique well region construction is provided.

DESCRIPTION OF DRAWING(S) - The figure shows the diagrammatic sectional view of semiconductor **wafer** fragment.

Substrate 12
Extension well region 14
p-type well region 16
p-type well **contact diffusion** region 38
Dwg.1/8

L11 ANSWER 2 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1999-287290 [24] WPIX
DNN N1999-214539
TI Electrostatic discharge (ESD) protection circuitry for VLSI **chip**
.
DC U13
IN LEE, J
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 1
PI US 5898205 A 19990427 (199924)* 6p
ADT US 5898205 A US 1997-891381 19970711
PRAI US 1997-891381 19970711
AB US 5898205 A UPAB: 19990624
NOVELTY - A capacitor (54) is added in a line between a Vss source and a Vcc source.

DETAILED DESCRIPTION - A CMOS FET (26) is connected between a Vss contact (16) and an I/O pad contact. Another CMOS FET (40) is connected between a Vcc contact and the I/O pad **contact**.
**Diffusions** in the VLSI **chip** form a first diode which turns ON when negative ESD stresses develop and form an NPN **transistor** and a second diode that turn ON when positive ESD

stresses develop. These stresses develop between the I/O pad contact and either the Vss contact or the Vcc contact.

USE - For VLSI **chips**.

ADVANTAGE - Enhances ESD protection.

DESCRIPTION OF DRAWING(S) - The drawing shows a diagrammatic illustration in section of a semiconductor device including the ESD protection circuit.

Vss contact 16
CMOS FET 26,40
capacitor 54
Dwg.2B/2

L11 ANSWER 3 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1996-505503 [50] WPIX
DNN N1996-425975
TI **Integrated circuit** with vertical Hall element - has device for isolating Hall device on epitaxial layer and position defining diffusion is formed of material of first conductivity type.
DC U12 U13
IN BIARD, J R
PA (HONE) HONEYWELL INC
CYC 1
PI US 5572058 A 19961105 (199650)* 19p
ADT US 5572058 A US 1995-503167 19950717
PRAI US 1995-503167 19950717
AB US 5572058 A UPAB: 19961211

The circuit includes a **transistor** emitter diffusion within the epitaxial layer. E.g. the **transistor** emitter diffusion has a depth of a second magnitude, which is less than that first. The **transistor** emitter diffusion comprising a material of the second conductivity type. A device is provided for isolating a Hall effect region of the epitaxial layer. A position defining diffusion includes a material of the first conductivity type, while the position defining diffusion has first, second, third, fourth and fifth openings formed in it.

The position defining diffusion is diffused within the epitaxial layer simultaneously with the **transistor** base diffusion. The first, second, third, fourth and fifth openings are disposed within the Hall effect region. First, second, third, fourth and fifth **contact diffusions** comprise a material of the second conductivity type and is diffused within the first, second, third, fourth and fifth openings, respectively.

USE/ADVANTAGE - For measuring strength of magnetic fields within epitaxial layer of silicon device. Provides relative high degree of accuracy in placement of these elements w.r.t. each other.

Dwg.4/9

L11 ANSWER 4 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1996-116448 [12] WPIX
CR 1995-090215 [12]
DNN N1996-097400 DNC C1996-036879
TI Contact structure to semiconductor material - comprises layer of silicide of first transition metal formed over semiconductor material, insulating layer over silicide layer, etc..
DC L03 U11 U12
IN CHIN, M; LIAO, K; WARREN, G
PA (HUGA) HUGHES AIRCRAFT CO
CYC 1
PI US 5491365 A 19960213 (199612)* 8p
ADT US 5491365 A CIP of US 1991-729243 19910712, Div ex US 1993-39718

19930329, US 1994-341795 19941118
FDT US 5491365 A Div ex US 5389575
PRAI US 1993-39718 19930329; US 1991-729243 19910712; US 1994-341795
19941118
AB US 5491365 A UPAB: 19960322
The contact structure to a semiconductor material consists of: (a) a layer (12) of a silicide of a first transition metal formed over the semiconductor material (4); (b) an insulating layer (16) formed over the silicide and having an opening; (c) a conductive contact extending through the opening; and (d) a layer (26) of **contact diffusion** -barrier material interposed between the contact and a portion of the silicide layer. The barrier layer is set into the silicide layer and the thickness of the silicide layer lateral to the opening is substantially equal to the combined thickness of the silicide layer and the barrier layer on the immediate vicinity of the opening. The barrier material is formed by implanting a second transition metal into the silicide layer.

Also claimed is a field effect **transistor** (FET).

USE - Used in mfg. semiconductor **integrated circuits** to prevent diffusion of the contact material into the underlying semiconductor.

ADVANTAGE - The improved diffusion barrier uses fewer processing steps, is less wasteful of barrier material and results in a barrier layer that is self-aligned with the contact opening.
Dwg.8/11

L11 ANSWER 5 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1994-219498 [27] WPIX
DNN N1994-173492
TI ESD device for circuit protection in BiCMOS **integrated circuit** esp. thick oxide ESD **transistor** - is formed only by steps for fabrication of BiCMOS **IC** protected circuitry, with polysilicon source-drain contacts and out-diffusion into source-drain regions, and e.g. uses BiCMOS collector reach through process for source-drain wells.
DC U13
IN FIORENZA, G; PELELLA, M M; SACCAMANGO, M J; YOUNG, R W
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 5
PI EP 604347 A2 19940629 (199427)* EN 17p
R: DE FR GB
JP 06232354 A 19940819 (199438) 13p
US 5504362 A 19960402 (199619) 14p
EP 604347 A3 19960110 (199620)
ADT EP 604347 A2 EP 1993-480215 19931203; JP 06232354 A JP 1993-317438 19931124; US 5504362 A Cont of US 1992-994739 19921222, US 1994-306532 19940914; EP 604347 A3 EP 1993-480215 19931203
PRAI US 1992-994739 19921222; US 1994-306532 19940914
AB EP 604347 A UPAB: 19940824
The ESD **transistor** is formed entirely by the BiCMOS **IC** mfg. process steps used in fabricating the internal protected circuitry, and occupies less than 100 square mum in area. The ESD device includes only one or more of the **IC** layers and dopant regions used in the BiCMOS **IC** protected circuitry. Pref. the ESD **transistor** source and/or drain contact includes part of either a base contact polysilicon layer or an emitter contact polysilicon layer formed in the protected circuit.

The ESD source or drain may be formed as an out-diffusion doping from its contact. The ESD **transistor** source or drain contact may be formed by a reach-through collector doping used in the protected circuit.

Pref. the ESD **transistor**, which may be a p-type or n-type
device, is formed in a CMOS well and has a gate electrode formed by a
bipolar **transistor** interconnection.
ADVANTAGE - Shunts up to 6kV; turn-on time of about 10ps, with higher
conductivity; increased current handling; no additional process steps.
Dwg.2/8

L11 ANSWER 6 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1993-205481 [25] WPIX
DNN N1993-157969
TI Radiation tolerant complementary MOS logic for **integrated circuit** - uses NMOS devices formed using lightly diffused P-well, and P-body diffusion having **contact diffusion** within body..
DC U11 U13 U21
IN HILL, K E; STEFURA, G A
PA (GENE) GENERAL ELECTRIC CO
CYC 1
PI US 5220218 A 19930615 (199325)* 10p
ADT US 5220218 A US 1991-763569 19910923
PRAI US 1991-763569 19910923
AB US 5220218 A UPAB: 19931116
The **integrated circuit** comprises a combination of a doubly diffused NMOS device in combination with PMOS device. The **integrated circuit** utilizes a P type substrate having a patterned N+ region formed therein and a lightly doped N type epitaxial layer formed thereon. P-channel MOS devices are formed using a lightly diffused N-well formed in the N type epitaxial layer.
The N-channel MOS (NMOS) devices are formed using a lightly diffused P-well formed in the same epitaxial layer. In accordance with the invention, an additional P-body diffusion having a doping concentration intermediate to that of the source **contact diffusion** and that of the P-well is provided. A P+/N+ **contact diffusion** formed within the P-body diffusion formed with the P-well completes the source and the P-well contact.
USE - Combining serially connected complementary metal oxide semi-conductor (MOS) active devices, Bi-polar **transistors**, and double diffused MOS power devices.
Dwg.1/6

L11 ANSWER 7 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1992-106485 [14] WPIX
DNN N1992-079814
TI Low voltage device in high voltage substrate - has thin gate dielectric of low voltage MOS **transistor** protected by depletion layer.
DC U13
IN AHRENS, M G; ELTOUKHY, A A; GALBRAITH, D C; ELTOUKHY, A
PA (ACTE-N) ACTEL CORP
CYC 15
PI EP 478123 A 19920401 (199214)* 5p
US 5286992 A 19940215 (199407) 5p
JP 06021354 A 19940128 (199409)
EP 478123 B1 19960925 (199643) EN 6p
R: AT BE CH DE ES FR GB GR IT LI LU NL SE
DE 69122342 E 19961031 (199649)
ADT EP 478123 A EP 1991-306667 19910722; US 5286992 A Cont of US 1990-590277 19900928, Cont of US 1992-865078 19920408, US 1993-38550 19930329; JP 06021354 A JP 1991-273405 19910925; EP 478123 B1 EP 1991-306667 19910722; DE 69122342 E DE 1991-622342 19910722, EP 1991-306667 19910722

FDT DE 69122342 E Based on EP 478123
PRAI US 1990-590277 19900928
AB EP 478123 A UPAB: 19931006
The semiconductor substrate of a first conducting has a well structure of a second conductivity. A first **transistor** gate lies above a channel region between source and drain regions of first conductivity type in a well of a first low voltage MOS **transistor**. A second **transistor** gate lies above a channel region between source and drain regions of a first conductivity type in the well of the second high voltage **transistor**.
A first **contact diffusion**, of the same conductivity type as the well, is located at the edge of the well closest to the low voltage **transistor**. A second **contact diffusion** of the same conductivity type is located at the edge of the well closest to the high voltage **transistor**. Both **contact diffusions** are connected to a source of voltage.
USE/ADVANTAGE - Method for incorporating low voltage MOS device in high voltage substrate or well.
1/3

L11 ANSWER 8 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1992-048494 [06] WPIX
DNN N1992-036867
TI Mixed technology **integrated circuit** - comprises CMOS structures and efficient lateral bipolar **transistors** with high early voltage.
DC U13
IN CONTIERO, C; GALBIATI, P
PA (SGSA) SGS-THOMSON MICROEL; (SGSA) SGS-THOMSON MICROEL
CYC 1
PI US 5081517 A 19920114 (199206)*
ADT US 5081517 A US 1990-548711 19900706
PRAI US 1990-548711 19900706
AB US 5081517 A UPAB: 20000630
The **integrated circuit** comprises CMOS structures and bipolar lateral **transistors**, the electrical efficiency and Early voltage of which are maintained high by forming ''well'' regions through the collector area. The operation determines the formation of a ''collector extension region'' extending relatively deep within the epitaxial layer so as to intercept the emitter current and gather it to the collector, subtracting it from dispersion toward the substrate through the adjacent isolation junctions surrounding the region of the lateral bipolar **transistor**.
Under comparable conditions, the ratio between IcIsubstrate is incremented from about 8 to about 300 and the Early voltage from about 20V to about 100V. The VCEO, BVCMO and BVCES voltages are also advantageously increased by the presence of the ''well'' region formed in the collector zone.
USE/ADVANTAGE - Mixed technology **integrated circuit** with exceptional versatility, used with increasing density in order to increase miniaturisation of the systems. @(6pp Dwg.No.3/3)@

L11 ANSWER 9 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1991-142053 [20] WPIX
DNN N1991-109353
TI **Integrated circuit** having MIS **transistor** - has **contact diffusion** regions in contact with power supply potential and gate electrode with resistance region connecting them.

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DC   U13
IN   SASAKI, M
PA   (SHIH) SEIKO EPSON CORP; (SHIH) SEIKO EPSON CO LTD
CYC  9
PI   EP 427565      A   19910515 (199120)*
         R: DE FR GB IT NL
     JP 03224270    A   19911003 (199146)
     US 5121179     A   19920609 (199226)       10p
     EP 427565      A3  19920304 (199325)
     US 5227327     A   19930713 (199329)       10p
     TW 230831      A   19940921 (199441)
     TW 273041      A   19960321 (199626)
     KR 164591      B1  19990115 (200037)
ADT  EP 427565 A EP 1990-312287 19901109; JP 03224270 A JP 1990-271555
     19901008; US 5121179 A US 1990-610620 19901108; EP 427565 A3 EP
     1990-312287 19901109; US 5227327 A Div ex US 1990-610620 19901108, US
     1992-819253 19920110; TW 230831 A TW 1992-107077 19901116; TW 273041 A TW
     1992-107078 19901116; KR 164591 B1 KR 1990-18159 19901110
FDT  US 5227327 A Div ex US 5121179
PRAI JP 1989-292627    19891110; JP 1990-271555   19901008
AB   EP     427565 A UPAB: 19931116
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The **integrated circuit** has at least one MIS **transistor** in which a gate electrode is arranged to be connected to a power supply potential through a protective resistor. A first **contact diffusion** region is formed within a semiconductor substrate or within a well in the semiconductor substrate and arranged to make contact with the power supply potential, and a second **contact diffusion** region is formed within the semiconductor substrate or the well as a position isolated from the first **contact diffusion** region and arranged in electrical contact with the gate electrode.

The region of the semi-conductor substrate or well between the first and second **contact diffusion** regions substantially constitutes a resistance region of the protective resistor. Generally, the impurity content of the semi-conductor substrate and the well therein is low and, as a result, the resistivity is high.

ADVANTAGE - Prevents breakdown of gate insulation film. @(11pp Dwg.No.1/5)@
1/5

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L11  ANSWER 10 OF 28  WPIX (C) 2002 THOMSON DERWENT
AN   1991-008484 [02]   WPIX
DNN  N1991-006666        DNC C1991-003710
```

TI   Mixed technology CMOS- bipolar **transistor IC** - process gives high electrical efficiency and early voltage.

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DC   L03 U13
IN   CONTIERO, C; GALBIATI, P; ZULLINO, L; GALBATI, P; ZUJLLINO, L
PA   (SGSA) SGS THOMSON MICROELTRN SRL; (SGSA) SGS-THOMSON MICROEL
CYC  8
PI   EP 405045      A   19910102 (199102)*
         R: DE FR GB IT NL SE
     JP 03054855    A   19910308 (199116)
     US 5081517     A   19920114 (199206)#
     EP 405045      B1  19951213 (199603)  EN    7p
         R: DE FR GB IT NL SE
     DE 68925116    E   19960125 (199609)
     US 35442       E   19970204 (199711)       8p
ADT  EP 405045 A EP 1989-830298 19890628; JP 03054855 A JP 1990-172529
     19900628; US 5081517 A US 1990-548711 19900706; EP 405045 B1 EP
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1989-830298 19890628; DE 68925116 E DE 1989-625116 19890628, EP 1989-830298 19890628; US 35442 E US 1990-548711 19900706, US 1994-183011 19940114

FDT DE 68925116 E Based on EP 405045; US 35442 E Reissue of US 5081517

PRAI EP 1989-830298 19890628; US 1990-548711 19900706

AB EP 405045 A UPAB: 20000712

A high-density, mixed technology **IC**, monolithically integrated in an epitaxial layer (2) of lightly doped Si, grown on a monocrystal line, lightly and oppositely doped Si (1) comprises complementary superficial FETs and bipolar lateral **transistors** of opposite polarity. Each of the latter is formed in an epitaxial region isolated from the substrate by a heavily doped buried layer (3) and isolated laterally by walls (4, 5B) of oppositely doped Si around the region. Each of the bipolar **transistors** comprises a heavily doped base **contact diffusion** region, an oppositely and heavily doped emitter diffusion and an oppositely and heavily doped annular collector around the emitter. These diffusions have identical profiles to respective source and drain regions of the CFETs and have a first and second annular opposite diffusion which contains the annular collector diffusion and extends beyond it, deeply within the epitaxial layer, for intercepting current from the emitter and gathering it to the collector, subtracting it from dispersion towards the isolation regions.

Pref. the bipolar **transistor** is PNP and the second annular diffusion formed in the collector zone has the same profile as a p-well used in an n-channel FET. Pref. a surface region of the second annular diffusion is B-enriched.

USE/ADVANTAGE - A mixed technology **IC** and method in which high density CMOS and lateral bipolar **transistors** having high early voltage and electrical efficiency are integrated is provided. The devices are very versatile in use. Early voltage is increased from 20 to 100 V and **Ic**/Isubstrate from 8 to 300 V(CEO), BV(CBO) and BV(CES) are also increased.

L11 ANSWER 11 OF 28 WPIX (C) 2002 THOMSON DERWENT

AN 1990-069108 [10] WPIX

DNN N1990-052896

TI Semiconductor **IC** device e.g. delay circuit for compact disc - has two **transistors** of same conductivity with adjacent, facing, source regions, receiving common power supply.

DC T03 U13 U22 W04

IN ASAMI, F; UDO, S

PA (FUIT) FUJITSU LTD; (KYUS-N) KYUSHU FUJITSU ELTRN LTD; (FUIT) KYUSHU FUJITSU ELECTRONICS KK

CYC 6

PI

| | | | | | |
|---|---|---|---|---|---|
| EP 357410 | A | 19900307 | (199010)* | EN | 37p |
| R: DE FR GB | | | | | |
| JP 02066958 | A | 19900307 | (199016) | | |
| JP 02066968 | A | 19900307 | (199016) | | |
| JP 02067004 | A | 19900307 | (199016) | | |
| EP 357410 | B1 | 19931103 | (199344) | EN | 41p |
| R: DE FR GB | | | | | |
| DE 68910445 | E | 19931209 | (199350) | | |
| KR 9308521 | B1 | 19930909 | (199433) | | |
| US 5391904 | A | 19950221 | (199513) | | 37p |

ADT EP 357410 A EP 1989-308798 19890831; JP 02066958 A JP 1988-216388 19880901; JP 02066968 A JP 1988-216387 19880901; JP 02067004 A JP 1989-216389 19890901; EP 357410 B1 EP 1989-308798 19890831; DE 68910445 E DE 1989-610445 19890831, EP 1989-308798 19890831; KR 9308521 B1 KR 1989-12672 19890901; US 5391904 A Cont of US 1989-400909 19890830, Cont of

US 1991-722353 19910618, US 1993-80651 19930622
FDT DE 68910445 E Based on EP 357410
PRAI JP 1988-216387 19880901; JP 1988-216388 19880901; JP 1988-216389 19880901
AB EP 357410 A UPAB: 19930928
The device includes pair of similar conduction type **transistors**, the source regions (21,21') of which are connected to a common power supply voltage (Vcc). The source regions are adjacent and face each other, but are separated by a substrate contact diffusing region (31) of opposite conductivity type which extends between ' the source regions and is of higher impurity density than the substrate.
The pairs of **transistors** may be formed by one **transistor** from each of two stocks of cascade connected inverter circuits forming a delay circuit. Each inverter circuit is formed by a P channel and an N channel **transistor** having P+ and N+ diffusion source regions (21,23) respectively.
ADVANTAGE - Prevents source current of one **transistor** affecting adjacent **transistor**.
6/26

L11 ANSWER 12 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1990-044934 [06] WPIX
DNN N1990-034466
TI **IC** semiconductor structure with reduced circuit spreading resistance - uses buries contact structure including diffusion dopant material and overlayed with poly silicon layer.
DC U11
IN EDWARDS, N P
PA (IBMC) IBM CORP
CYC 1
PI US 4885627 A 19891205 (199006)* 7p
ADT US 4885627 A US 1988-259473 19881018
PRAI US 1988-259473 19881018
AB US 4885627 A UPAB: 19930928
The buried contact structure includes a phosphorous diffusion superimposed on the field implant which includes the source and/or drain of an NMOS **transistor**. An overlayed layer of polysilicon is disposed to make contact with the buried **contact diffusion**. The field implant used for the source and drain may, for example, be boron, and have a resistance of 15 to 20 Ohms per square.
Electron current flows from source to drain through a channel under the gate, then through a depletion implant under a load gate to a contact and the supply bus. Current is controlled by voltage applied to polysilicon control gate. The buried contact structure which has a lower resistance than the field implant is used.
USE/ADVANTAGE - Decreases spreading resistance of varioius circuit elements of semiconductor devices such as **transistors** and reduces resistance of polysilicon wires typically used in short lengths to connect circuit elements to other metallic wires. For high speed, high power applications. Can be used for NMOS or CMOS.
7/7

L11 ANSWER 13 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1989-124346 [17] WPIX
DNN N1989-094783 DNC C1989-055126
TI Saturation-limiting system - is for vertical isolated PNP **transistor**, has monolithically integrated structure.
DC L03 P14 U12 U13
IN BERTOTTI, F; FERRARI, P; GATTI, M T

PA (SGSA) SGS-THOMSON MICROEL; (SHES) SGS-THOMSON MICROEL; (SGSA) SGS
MICROELETTRONICA SPA
CYC 6
PI EP 313526 A 19890426 (198917)* EN 6p
R: DE FR NL
JP 01129458 A 19890522 (198926)
US 4887141 A 19891212 (199007) 4p
IT 1220185 B 19900606 (199214)
EP 313526 B1 19930519 (199320) EN 6p
R: DE FR NL
DE 3881148 G 19930624 (199326)
ADT EP 313526 A EP 1988-830424 19881018; JP 01129458 A JP 1988-265211 19881020; US 4887141 A US 1988-260236 19881019; IT 1220185 B IT 1987-83666 19871021; EP 313526 B1 EP 1988-830424 19881018; DE 3881148 G DE 1988-3881148 19881018, EP 1988-830424 19881018
FDT DE 3881148 G Based on EP 313526
PRAI IT 1987-83666 19871021
AB EP 313526 A UPAB: 19930923
A monolithically integrated vertical PNP **transistor** with isolated collector formed in an n-type epitaxial layer (2) grown on a monocrystalline Si substrate comprises the following components:- (1) a buried p+-type collector ayer (C), contactable from the surface through a p+-type sinker diffusion, completely surrounding a base region of the **transistor**, and bounded by the collector layer and by the sinker diffusion, (2) a p-type emitter diffusion (5,6) and an n-type base **contact diffusion**, both contained within the base region, and (3) an isolation p+-type diffusion, extending through the whole thickness of the epitaxial layer, surrounding the entire area of the **transistor**. A p- or p+-type diffusion is formed in the epitaxial layer, in a zone between the collector/sinker- and isolation-diffusion; the p- or p+-type diffusion forms an auxiliary collector region of the integrated **transistor**.

The auxiliary collector is idependently connectable from the collector of the **transistor** to an input terminal of an antisaturation circuit. This circuit can reduce a driving base current of the integrated **transistor**; when excessive saturation of the integrated **transistor** occurs, the auxiliary collector gathers a portion of a preset value of a total leakage current injected towards the substrate by the satd. PNP **transistor**.

USE/ADVANTAGE -Applicable to **integrated circuits**; partic. power output stages. Permits the realisation of a more efficient antisaturation system than prior art systems.
2,3/3

L11 ANSWER 14 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1989-072979 [10] WPIX
TI Bipolar-CMOS power **transistor** with ultra-low ON resistance - has channel and source regions at one side of insulated gate and drain diffused region at other side NoAbstract Dwg 8/10.
DC U12
IN YASUOKA, H
PA (HITA) HITACHI LTD
CYC 2
PI JP 01025574 A 19890127 (198910)* 4p
US 5256893 A 19931026 (199344)B 14p
ADT JP 01025574 A JP 1987-181101 19870722; US 5256893 A Cont of US 1988-221372 19880719, Cont of US 1990-528897 19900529, Cont of US 1991-779855 19911021, US 1992-995051 19921222
PRAI JP 1987-181101 19870722

AB US 5256893 A UPAB: 19931213 ABEQ treated as Basic
The vertical power MOSFET has a gate electrode with a number of polysilicon film electrode strips formed on an n- epitaxial silicon layer on the surface of a p- semiconductor substrate and insulated from the epilayer by an insulating film. An n+ diffusion layer, to contact the drain, is located within the n- epitaxial layer at a region corresp. to two adjacent gate electrode strips.

A p-type diffused layer which contains a channel region, and an n+ diffused source layer are formed around each of the two adjacent gate electrode strips.

USE/ADVANTAGE - For esp. mixed bipolar **transistor** and power MOSFET **IC**, with low MOSFET on resistance due to parasitic drain resistance, with close channel and drain **contact diffusion** spacing. Reduced heat generation; self-aligned drain lead-out region.
Dwg.1/9

L11 ANSWER 15 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1988-007741 [02] WPIX
DNN N1988-005447 DNC C1988-003451
TI Vertical bipolar **transistor** construction in silicon **IC** - forms deep collector contacts and emitters simultaneously to allow increased packing density.
DC L03 U11 U13
IN ROLOFF, H F
PA (SIEI) SIEMENS AG
CYC 1
PI DE 3621179 A 19880107 (198802)* 4p
ADT DE 3621179 A DE 1986-3621179 19860625
PRAI DE 1986-3621179 19860625
AB DE 3621179 A UPAB: 19930923
On the p-type substrate (1) buried layers (2.1 and 2.2) are formed of n-type substrate, pref. by implantation of 10 power 14 to 10 power 15 ats. Sb/cm2, and diffused. One of these layers is formed for each of the **transistor** types. Further p-type implants are then made (3.2.4.1), pref. of 10 power 14 to 4 x 10 power 14 ats. B/cm2, followed by a further B-implant (3.1) for the collector of 1.5-4 x 10 power 13 ats /cm2.

An n-type epitaxial layer (5) is then deposited, of e.g. 0.5-3 ohmcm. P-type implants 3.3, 4.2) are made in the corresponding places in the epitaxial layer surface which make contact with the buried layers diffusion fronts (3.2, 4.1). An n-type implant then is made to form the emitter (8) of the npn-**transistor**.

The feature is claimed both for pnp-**transistors** on p-type substrate and for npn-**transistors** on n-type substrate.

USE/ADVANTAGE - The process reduces the distance between emitter and deep collector **contact diffusion** at the surface of the epitaxial layer. This can cause an area reduction of 10%. It is used to mfr. bipolar **integrated circuits**.
2/3

L11 ANSWER 16 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1987-300307 [43] WPIX
DNN N1987-224348 DNC C1987-127756
TI Buried contact structure in **IC** devices - includes a **contact diffusion** superimposed on a **transistor** element.
DC L03 U12
IN EDWARDS, N P
PA (IBMC) IBM CORP

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CYC  13
PI   EP 242540      A  19871028 (198743)* EN     7p
         R: CH DE ES FR GB IT LI NL SE
     AU 8771732     A  19871022 (198749)
     JP 62252173    A  19871102 (198749)
     BR 8701660     A  19880112 (198808)
     CA 1285663     C  19910702 (199147)
ADT  EP 242540 A EP 1987-102788 19870227; JP 62252173 A JP 1987-49016 19870305
PRAI US 1986-854283    19860421
AB   EP     242540 A UPAB: 19930922
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**IC** structure comprises: a semiconductor substrate; a first layer of conductive semiconductor material formed on the substrate to form a **transistor** source; a second similar layer forming a drain; a third similar layer forming a gate; and a buried contact structure superimposed on the first and/or second layers formed of diffusion material and on an overlayed polySi layer. The **contact diffusion** material has a lower resistance than that of the **transistor** element.

ADVANTAGE - The spreading resistance of the source/drain and polySi wire elements is reduced; resistance is reduced in circuits such as power drivers for dynamic latches.

1/4

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L11  ANSWER 17 OF 28  WPIX (C) 2002 THOMSON DERWENT
AN   1987-229461 [33]   WPIX
DNN  N1987-171774        DNC C1987-096712
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TI Simultaneous integration of CMOS- and self-aligned bipolar- **transistors** - produces circuits for high frequency operation.

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DC   L03 U11 U13
IN   SCHABER, H; SCHABER, H C
PA   (SIEI) SIEMENS AG
CYC  8
PI   EP 232497      A  19870819 (198733)* DE     8p
         R: AT DE FR GB IT NL
     JP 62155552    A  19870710 (198733)
     US 4735911     A  19880405 (198816)         6p
     EP 232497      B1 19930310 (199310)  DE    10p
         R: AT DE FR GB IT NL
     DE 3687973     G  19930415 (199316)
ADT  EP 232497 A EP 1986-116737 19861202; US 4735911 A US 1986-931641 19861117;
     EP 232497 B1 EP 1986-116737 19861202; DE 3687973 G DE 1986-3687973
     19861202, EP 1986-116737 19861202
FDT  DE 3687973 G Based on EP 232497
PRAI DE 1985-3544638   19851217
AB   EP     232497 A UPAB: 19930922
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In the p-type substrate (Si) n-type areas (2) are implanted and diffused to form buried layers. A p- or n-type epitaxial layer is then grown, a double layer of Si-oxide and -nitride deposited and defined and the S- **wafer** subjected to an oxidation. This forms field-oxide areas (6). Then n-type areas (5) or p-type areas (3) depending on the type of epitaxial layer deposited before, as well as the collector **contact -diffusions** (4) are implanted and diffused. The oxidation masking layer is then removed and a B-doped polysi, silicide or polycide layer (7) from which the base-contacts and p-channel source/drain-region are formed, is deposited followed by an insulating layer (8). A photoresist process-step is used to define the bipolar **transistor** base-area and the source/drain areas of the p-channel MOS- **transistors** (C) using a dry etch-process to produce steep edges to the features defined. Using photoresist as a mask the base-region (9) is then implanted with B-ions. An insulating layer, e.g. not SiO2, is then

deposited to give good edge-coverage of the polysi-features (7). An anisotropic etching process then removes this oxide again except on the edges mentioned (10). Then an n+-type layer (11), of polysi silicide or polycide is deposited to form source/drain area of the p-channel MOS (C) and the emitter/collector-contacts of the bipolar **transistor** (A). The gate-areas are then etched free and the thickness of the oxide on the edges (10,12) of the source/drain doping sources (7,11) adjusted to give the required channel-length. The gate-oxide (17) is then regrown and the channel-threshold adjusted by a B-implant.The the gate-electrode-layer is deposited, doped and the pattern (18,19) defined. An insulating oxide layer (20) is deposited, contact windows are opened and metallisation is carried out to complete the circuits in the standard way.
5/5

L11 ANSWER 18 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1986-052628 [08] WPIX
TI Process for mfg. semiconductor **IC** with insulated gate FET - comprises forming gate electrodes, wiring and its contacts in diffused layers forming two layers of photoresist patterns NoAbstract Dwg 2/2.
DC L03 U11 U12
PA (NIDE) NEC CORP
CYC 1
PI JP 61006865 A 19860113 (198608)* 13p
ADT JP 61006865 A JP 1984-126796 19840620
PRAI JP 1984-126796 19840620

L11 ANSWER 19 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1983-784591 [41] WPIX
DNN N1983-179461
TI Monolithic integrated power circuit - uses heavy-current PNP **transistor** with two insulating P-type walls between which NPN **transistor** is formed.
DC U11 U13
IN VANZENTEN, F
PA (CSFC) THOMSON CSF
CYC 5
PI EP 90686 A 19831005 (198341)* FR 14p
    R: DE FR GB NL
  FR 2523370 A 19830916 (198342)
  EP 90686 B 19860108 (198603) EN
    R: DE FR GB NL
  US 4564855 A 19860114 (198605)
  DE 3361745 G 19860220 (198609)
ADT EP 90686 A EP 1983-400426 19830302; US 4564855 A US 1983-473672 19830308
PRAI FR 1982-4216 19820312
AB EP 90686 A UPAB: 19930925
Successive epitaxial layers (2,3) of types P and N-are deposited on a substrate (1) of N+ type and the PNP **transistor** (T1) comprises a central zone (10) bounded by peripheral insulating walls (11,12) of P-type material, projecting through the second epitaxial layer (3) into the first layer (2). Its emitter (13) and base (14) regions (E1,B1) are formed in the surface, and the inner wall (11) is overlaid with a collector metallisation (C1).

A continuous peripheral ring (21) of N+ type is bured between the two walls and extends from the substrate (1) into the second layer (3) locally short-circuiting the P layer (2) and isolating its central part. The NPN **transistor** (T2) is formed between the walls (11,12) with a N-type emitter region (23) within a P-type base region (22).
4/5

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L11  ANSWER 20 OF 28  WPIX (C) 2002 THOMSON DERWENT
AN   1983-D4559K [10]   WPIX
DNN  N1983-045465
TI   IC diode with reduced substrate leakage - has annular,
     heavily-doped region surrounding layer and contacting second,
     heavily-doped bottom diffusion.
DC   U12
PA   (EKLU-I) EKLUND K H; (TELF) TELEFONAKTIEBOLAGET ERICSSON L M
CYC  11
PI   WO 8300776    A  19830303 (198310)* EN   10p
        RW: DE FR GB NL
         W: DK FI NO US
     SE 8105040    A  19830328 (198315)
     NO 8301436    A  19830620 (198331)
     EP 86210      A  19830824 (198335)  EN
         R: DE FR GB NL
     DK 8301793    A  19831128 (198403)
     FI 8301227    A  19831130 (198403)
     JP 59158568   A  19840908 (198442)
     EP 86210      B  19850710 (198528)  EN
         R: DE FR GB NL
     DE 3264667    G  19850814 (198534)
     IT 1207305    B  19890517 (199132)
ADT  EP 86210 A EP 1982-902481 19820819; JP 59158568 A JP 1983-30184 19830224
PRAI SE 1981-5040     19810825
AB   WO    8300776 A UPAB: 19930925
     The diode cathode (18,23) is formed in the epitaxial n-collector layer
     (15) of the circuit. The anode is a p+ bottom layer (13) situated under
     this collector layer and produced simultaneously with the lower portion of
     the isolation diffusion (14). The cathode region  (23) is defined by a
     ring (17) of the same conduction type as the bottom layer (13) and makes
     contact with it.
          Under the bottom layer there is an n+ type buried sub-collector layer
     (12) provided with a contact diffusion (19) of the
     same conduction type. The anode layer (13) and sub-collector layer (12)
     are then mutually connected at low resistance.
     1/3

L11  ANSWER 21 OF 28  WPIX (C) 2002 THOMSON DERWENT
AN   1983-D4558K [10]   WPIX
DNN  N1983-045464
TI   Planar transistor with integrated overvoltage guard - has Zener
     diode between collector and base and contact diffusion
     extending over barrier layer.
DC   U12 U13 U21 U24
PA   (EKLU-I) EKLUND K H; (TELF) TELEFONAKTIEBOLAGET ERICSSON L M
CYC  7
PI   WO 8300775    A  19830303 (198310)* EN   10p
        RW: DE FR GB
         W: JP US
     SE 8105041    A  19830328 (198315)
     EP 86209      A  19830824 (198335)  EN
         R: DE FR GB
     JP 58501352   W  19830811 (198338)
     IT 1152086    B  19861224 (198850)
PRAI SE 1981-5041     19810825
AB   WO    8300775 A UPAB: 19930925
     An overvoltage guard is connected between the collector (17) and base (19)
```

and integrated in the same semiconductor **wafer** (16) as the **transistor**. The guard comprises a Zener diode formed between the collector and a portion of a **contact diffusion** (23) formed in the base electrode and having a higher degree of doping than the base. The **contact diffusion** extends over the base-collector barrier layer - partly or wholly.

The **contact diffusion** (23) can extend so far into the collector region and the diffusion conditions be so selected that the barrier layer (26) between the **contact diffusion** and the collector layer (17) is given a radius of curvature corresp. to the desired breakdown voltage of the Zener diode.

2/6

L11 ANSWER 22 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1981-G6236D [29] WPIX
TI Voltage distribution system of LSI **chip** - uses polycrystalline grid with direct contact to diffused electrodes to reduce ground resistance.
DC U11 U13
IN DELAMONEDA, F; WILLIAMS, T
PA (IBMC) IBM CORP
CYC 4
PI EP 31539 A 19810708 (198129)* EN 19p
    R: DE FR GB
   US 4458406 A 19840710 (198430)
   EP 31539 B 19870325 (198712) EN
    R: DE FR GB
   DE 3071936 G 19870430 (198718)
ADT EP 31539 A EP 1980-107938 19801216; US 4458406 A US 1981-310337 19811009
PRAI US 1979-108074 19791228; US 1981-310337 19811009
AB EP 31539 A UPAB: 19930915

The system consists of polycrystalline material columns (28) of the same conductivity type as the semiconductor body (10). The columns intersect a set of polycrystalline material rows (32). The number of columns and rows and their respective periodicities need not be the same. The columns and rows are provided with metallic connections to perimeter pads. The rows and columns cover, partially or completely, the holes through the insulating layer (12,16) so as to form an electrical contact with first regions (22) of the other conductivity type.

The system is useful for large scale arrays of **integrated circuits**. **Chip** performance is enhanced by the use of vertical structures. The distribution bus for MOSFET LSI **chips** is provided without increasing fabrication complexity. The system is incorporated into the ROM by modifying the conventional double polysilicon process for making one-**transistor** memory cells. An extra masking-etching operation opens the through holes in the oxide-covered row regions.

1D,1E

L11 ANSWER 23 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1979-38949B [20] WPIX
TI Silicon base CCD-bipolar **transistor** - produced by applying perforated mask to **chip** and etching to form silicon di oxide mask.
DC L03 U12 U13
IN WANG, C S
PA (USSA) US SEC OF ARMY
CYC 1
PI US 4152715 A 19790501 (197920)*

PRAI US 1977-855514 19771128
AB US 4152715 A UPAB: 19930901
CCDs and bipolar **transistors** are formed together on a silicon **chip**. For n channel CCDs and npn **transistors**, only a single extra diffusion is necessary in addition to the diffusions used for the CCDs alone. This step is diffusion of n+ collector wells, and is performed before CCD channel stop-**transistor** base diffusion.
For p channel CCDs and pnp **transistors**, two extra diffusions are necessary and are: diffusion of a p collector wells, and diffusion of n+ base contracts.
The extra diffusions may both be performed before CCD channel stop **transistor** base diffusion, or the n+ base **contact diffusion** may be performed after that.

L11 ANSWER 24 OF 28 WPIX (C) 2002 THOMSON DERWENT
AN 1979-11255B [06] WPIX
TI Semiconductor prodn. - by inserting deep resistance layer between base **contact diffusion** layer and base layer.
DC L03 U12
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 54000755 B 19790116 (197906)*
JP 50011585 A 19750206 (197906)
PRAI JP 1973-61121 19730531
AB JP 79000755 B UPAB: 19930901
A deep resistance layer having a specified concn. and a deep diffusion depth is inserted between a base **contact diffusion** layer and a proper base layer having the same electro-conductivity as that of the resistance.
Prod. is combined with hypola-**transistor** having **integrated circuit**.

L11 ANSWER 25 OF 28 JAPIO COPYRIGHT 2002 JPO
AN 2001-177061 JAPIO
TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD
IN GOTO HIROYOSHI
PA NEC IC MICROCOMPUT SYST LTD
PI JP 2001177061 A 20010629 Heisei
AI JP1999-357055 (JP11357055 Heisei) 19991216
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To mix memory circuits, **logic circuits**, or **logic circuits** in high density in a semiconductor device, by enabling a large capacity of capacitive element required for a semiconductor device to be effectively formed within a semiconductor **chip**.
SOLUTION: In a semiconductor device which is composed of a semiconductor element including an insulated gate field effect **transistor**, well layers 2 and 3 are made on the surface of a semiconductor substrate (silicon substrate 1), gate electrodes 6 and 7 are made through a gate insulating film on these well layers, **contact diffusion** layers 4 and 5 of the same conductivity type as the well layers are made on the surfaces of the well layers across gate electrodes, and a capacitive element which makes the gate electrode one electrode, the well layer and the diffusion layers the counter electrodes, and the gate insulating film a capacitive insulating film is made. Moreover, a region which includes impurities in higher concentration than the well layer and of the same conductivity type as it is made on the surface of the well layer under the gate electrode.

L11 ANSWER 26 OF 28 JAPIO COPYRIGHT 2002 JPO
AN 1995-153927 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT**
IN KUMAGAI KOICHI
PA NEC CORP, JP (CO 000423)
PI JP 07153927 A 19950616 Heisei
AI JP1993-301392 (JP05301392 Heisei) 19931201
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 6
AB PURPOSE: To prevent deterioration of the circuit operating speed by causing the source and drain diffusion construction of a fundamental cell to have LDDs and asymmetrical CMOS **transistors**.
CONSTITUTION: Concerning a fundamental cell 103, three P-type MOS **transistors** 108a-108c from A side being the side of a well **contact diffusion** layer and three N-type MOS **transistors** 109a-109c from B-side are all formed by the use of asymmetrical LDD **transistors** respectively. And the remaining each one **transistor**, a P-type MOS **transistor** 108d and an N-type MOS **transistor** 109d, is formed using an LDD **transistor** having a symmetrical construction. Accordingly, on-current increases compared to conventional layout, and load drivability can be enhanced, especially at rise time, since two asymmetrical LDD **transistors** are connected in parallel.

L11 ANSWER 27 OF 28 JAPIO COPYRIGHT 2002 JPO
AN 1991-019236 JAPIO
TI BIPOLAR **TRANSISTOR**
IN SHIMIZU KEIICHIRO
PA MATSUSHITA ELECTRON CORP, JP (CO 000584)
PI JP 03019236 A 19910128 Heisei
AI JP1989-153452 (JP01153452 Heisei) 19890615
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1053, Vol. 15, No. 139, P. 99 (19910409)
AB PURPOSE: To improve mutual conductance by arranging a second conductivity type base region and a first conductivity type drain region in a first conductivity type collector region, and electrically connecting a source region, a substrate region, and an emitter region.
CONSTITUTION: A P-type well 2 is formed on an epitaxial layer 1; after a gate insulating film 3 is formed, polysilicon is deposited on the surface of a **wafer**, and impurity is added to the silicon film, thereby turning it into a sheet resistor; by selectively etching the polysilicon film, a gate electrode 4 is formed, and by ion implantation, a P+ type base diffusion layer 5 is formed; by ion implantation, an N+ type collector **contact diffusion** layer 6, an N+ type emitter diffusion layer 7, an N+ type source diffusion layer 8, and an N+ type drain diffusion layer 9 are formed; an interlayer insulating film 10 is formed; a contact window is made; by using aluminum, a base gate.cntdot.common electrode 11, an emitter electrode 12, a collector electrode 13, and a source substrate electrode 14 are formed. Thereby current characteristics can be improved.

L11 ANSWER 28 OF 28 JAPIO COPYRIGHT 2002 JPO
AN 1983-213446 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT**
IN ASANO TETSUO; TABATA TERUO
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
TOKYO SANYO ELECTRIC CO LTD, JP (CO 323368)
PI JP 58213446 A 19831212 Showa

AI JP1982-96658 (JP57096658 Showa) 19820604
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 233, Vol. 8, No. 631, P. 113 (19840324)
AB PURPOSE: To prevent a thyristor parasitic effect by forming a through diffusion region of high impurity concentration into a third island region.

CONSTITUTION: An N type epitaxial layer 12 is formed onto a P type semiconductor substrate 11. The epitaxial layer 12 is P-N isolated into island regions 13, 14, 15 by a P+ type isolation region 16. A P+ type diffusion region 17 is formed to the surface of the first island region 13. A **transistor** region 20 consisting of a P type base region 18 and an N+ type emitter region 19 is formed to the surface of the second island region 14. The third island region 15 is formed independently between the first and second island regions 13, 14. The through diffusion region 21 is formed to the third island region 15 by an N+ type buried layer 211 in the bottom, an N+ type collector **contact diffusion** layer 212, which is diffused from the surface and reaches the buried layer 211, and an N+ type diffusion region 213 by emitter diffusion.

L16 ANSWER 1 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 2002-291341 [33] WPIX
DNN N2002-227476 DNC C2002-085427
TI Complementary metal oxide semiconductor **transistor** device used in **integrated circuits**, includes N-type and P-type **transistors**, in which buried layers are grounded and biased at positive supply voltage.
DC L03 U11 U13
IN DOYLE, B R
PA (INTE-N) INTERSIL AMERICAS INC
CYC 1
PI US 2002020858 A1 20020221 (200233)* 8p
ADT US 2002020858 A1 Provisional US 2000-223847P 20000808, US 2001-918208 20010730
PRAI US 2000-223847P 20000808; US 2001-918208 20010730
AB US2002020858 A UPAB: 20020524
NOVELTY - A complementary metal oxide semiconductor (CMOS) **transistor** device comprises a substrate of a first **conductivity type**. N-type MOS and P-type MOS **transistors** are formed within respective first and second **well regions**, in which the buried layer having the NMOS **transistor** is grounded and the buried layer having the PMOS **transistor** is biased at a positive supply voltage.
DETAILED DESCRIPTION - A complementary metal oxide semiconductor (CMOS) **transistor** device comprises a substrate (16) of a first **conductivity type**. First and second buried layers are formed within the substrate, and has a second **conductivity type** opposite from the first. First and second **well regions** of first and second conductivity are formed above respective first and second buried layers. An NMOS **transistor** and PMOS **transistor** are formed within respective first and second **well regions**, in which the buried layer having the NMOS **transistor** is grounded and the buried layer having the PMOS **transistor** is biased at a positive supply voltage to improve single event effects occurrence.

L16 ANSWER 2 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 2002-178734 [23] WPIX
CR 2002-065671 [06]
DNN N2002-135901 DNC C2002-055310
TI **Integrated circuit** includes a sacrificial conductive path which temporarily couples the gate of a capacitor structure to the semiconductor substrate to discharge any charge accumulation.
DC L03 U12
IN WILFORD, J R
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6342723 B1 20020129 (200223)* 12p
ADT US 6342723 B1 US 1999-295988 19990421
PRAI US 1999-295988 19990421
AB US 6342723 B UPAB: 20020411
NOVELTY - **Integrated circuit** (10) includes a sacrificial conductive path (32) which temporarily couples the gate (26) of a capacitor structure to the semiconductor substrate (12) to discharge any charge accumulation. The sacrificial area (34) is removed prior to operation of the device to sever the connection between the gate and the substrate.
DETAILED DESCRIPTION - **Integrated circuit**

comprises:
(a) a substrate (10) of a first **conductivity type**
;
(b) a **well region** formed in the substrate of a second **conductivity type** opposite the first **conductivity type**;
(c) a capacitive structure formed on the substrate, the capacitive structure consisting of an insulating layer (22) between the substrate and a conductive layer;
(d) a conductive path (32) coupling the conductive layer to the substrate through a **doped region** formed in the substrate. The conductive path has a removable portion to decouple the conductive layer from the substrate when removed.

L16 ANSWER 3 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 2002-081592 [11] WPIX
DNN N2002-060678 DNC C2002-024564
TI A high voltage MOS **transistor** reduces the snap back phenomenon.
DC L03 U11 U12
IN TUNG, M
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 2
PI TW 441030 A 20010616 (200211)*
US 6392274 B1 20020521 (200239)#
ADT TW 441030 A TW 2000-106046 20000331; US 6392274 B1 US 2000-542842 20000404
PRAI TW 2000-106046 20000331; US 2000-542842 20000404
AB TW 441030 A UPAB: 20020215
NOVELTY - The present invention provides a HVMOS **transistor** fabricated on a semiconductor **chip**. The semiconductor **chip** includes a silicon substrate of the first **conductive type** and a silicon epitaxy layer of the second **conductive type** formed on the surface of the silicon substrate. The HVMOS includes the first **doped well region** of the second **conductive type** formed on the surface of the silicon epitaxy layer, the second **doped well region** of the second **conductive type** formed on the first **doped well region**, a source region of the first **conductive type** formed on the second **doped well region**, a drain region of the first conductive region formed in the silicon epitaxy layer, a gate and a diffusion region of the second **conductive type** formed in the silicon epitaxy layer right under the first **doped well region** and the silicon substrate, and the diffusion region has partial overlapping with the first **doped well region**.
Dwg.0/1

L16 ANSWER 4 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 2001-450925 [48] WPIX
DNN N2001-333826
TI Electrostatic discharge protection circuit for semiconductor **chip**, has substrate, **well region**, first **doping region** and second **doping region**..
DC U13 U21 U24
IN CHEN, W
PA (WINB-N) WINBOND ELECTRONICS CORP
CYC 1
PI US 2001007521 A1 20010712 (200148)* 21p
ADT US 2001007521 A1 US 2000-747209 20001222

PRAI TW 2000-100331 20000111
AB US2001007521 A UPAB: 20010829
NOVELTY - The electrostatic discharge (ESD) protection circuit has a substrate, a **well region** with a first **conductivity type**, a first **doping region** and second **doping region**.
DETAILED DESCRIPTION - The ESD protection circuit is coupled between a reference potential and a semiconductor **chip** circuit node. The substrate is coupled to the reference potential. The **well region** has a second **conductivity type**, and is formed on the substrate. This is coupled to the node. The first **doping region** also has a first **conductivity type**, and is electrically floated on the **well region**. The second **doping region** has the second **conductivity type**, and is located on the substrate. This is electrically coupled to the reference potential. The operation is such that when the ESD current of the node provides a voltage with sufficient magnitude to breakdown the interface between the well and the substrate, then a bipolar junction **transistor** (BJT) is triggered. The BJT comprises the **well region**, the substrate and the second **doping region**. This action dissipates the ESD current. Also, the first **doping area** acts to reduce the potential difference between the node and the reference.
USE - For semiconductor **chip**.
ADVANTAGE - Provides ESD protection circuit with high triggering current and low holding current. Uses a very small area of the semiconductor **chip**.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic sectional diagram illustrating the ESD protection circuit.
Node 10
Substrate 12
**Well region** 14
First **doping region** 16
Second **doping region** 18
Third **doping region** 20
Fourth **doping region** 22
Dwg.1/14

L16 ANSWER 5 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1999-048209 [05] WPIX
DNN N1999-035324 DNC C1999-015329
TI SRAM cell with thin-film pull-up **transistors** - with reduced memory cell area.
DC L03 U11 U12 U13 U14
IN BRYANT, F R; CHAN, T C
PA (SGSA) STMICROELECTRONICS INC; (SGSA) SGS THOMSON MICROELTRN INC
CYC 27
PI EP 887857 A1 19981230 (199905)* EN 15p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 11074378 A 19990316 (199921) 11p
US 6140684 A 20001031 (200057)
US 6271063 B1 20010807 (200147)
ADT EP 887857 A1 EP 1998-304874 19980619; JP 11074378 A JP 1998-177688 19980624; US 6140684 A US 1997-881342 19970624; US 6271063 B1 Div ex US 1997-881342 19970624, US 2000-593334 20000614
PRAI US 1997-881342 19970624; US 2000-593334 20000614
AB EP 887857 A UPAB: 20001109

A method of producing a static random access memory (SRAM) semiconductor device structure with thin film pull-up **transistors** comprises forming field isolation regions within an active **well region** of a first **conductivity type** formed in a semiconductor substrate. A first polysilicon (poly 1) gate stack, including a gate oxide, a first polysilicon silicide and an oxide, is formed and patterned in a desired manner, wherein the first polysilicon and silicide form appropriate gate electrodes for bulk silicon **transistor** devices of a second **conductivity type** to be formed in the substrate. Lightly **doped** drain (LDD) **regions** of the second **conductivity type**, oxide sidewall spacers, and source/drain regions of the second **conductivity type** are formed. A second gate oxide for the yet to completed thin film pull-up **transistors** (TFTs) is formed, and shared contact regions in the second gate oxide are patterned and etched. A second polysilicon (poly 2) is deposited to be used for an active area to poly 1 interconnect strap, Vcc, and for channel regions of the yet to be completed first **conductivity type** channel TFTs. Ions of a first **conductivity type** implanted for adjusting a threshold voltage Vt of the yet to be completed first **conductivity type** channel TFTs. A Vcc/source-drain and shared contact areas of the poly 2 are patterned,and implanted with ions of a first **conductivity type**, wherein the implant includes a highly doped implant for the TFTs which extends close to an active/gated source area TFT, and wherein a gate electrode of the TFTs is formed by a substrate storage node side of a second **conductivity type** channel pull-down **transistors** formed in the substrate. Second-polysilicon shared contacts and a Vcc trace are patterned and etched, wherein poly 2 stringers are created, along side edges of the poly 1 patterned gate stack. A stringer removal mask is patterned for protecting desired poly 2 stringers along side edges of the poly 1 patterned gate stack, and undesired poly 2 stringers removed by etching, wherein the remaining poly 2 stringers form the channel regions of the TFTs. A dielectric material is deposited and back-end interconnect processing continued.

USE - Methods of making semiconductor **integrated circuit** structures, particularly SRAM cells.

ADVANTAGE - Reduced memory area (10-20 mu m2) while avoiding performance degradation.

Dwg.4/5

L16 ANSWER 6 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1997-258222 [23] WPIX
CR 1997-033647 [03]
DNN N1997-213603
TI Lateral bipolar **transistor** formation method for BiCMOS VLSI - using direct self aligned poly silicon contacts to base region and to emitter and collector **regions** and heavily **doped** buried layers.
DC U11 U13
IN LI, X; VOINIGESCU, S P
PA (NELE) NORTHERN TELECOM LTD
CYC 1
PI US 5624856 A 19970429 (199723)* 9p
ADT US 5624856 A Div ex US 1995-546642 19951023, US 1996-662964 19960613
PRAI US 1995-546642 19951023; US 1996-662964 19960613
AB US 5624856 A UPAB: 19970606
The method of forming a lateral bipolar **transistor** (30) includes providing an **integrated circuit** substrate (32) with

two heavily doped buried layers (34,36) of opposite **conductivity type**. **Well regions** (38,40) of corresponding **conductivity type** are formed on the buried layers. Field isolation regions (42) are defined on the substrate with openings defining **well regions**. A heavily **doped** polysilicon layer (56) is formed on the substrate. A dielectric isolation layer (54) is provided on the first polysilicon layer. The first polysilicon and overlying dielectric layers are patterned to define a base contact opening and the two polysilicon layers form a collector contact electrode and an emitter contact electrode adjacent the base contact opening.

Dielectric sidewall spacers (60) are provided on sidewalls of the polysilicon layer within the base contact opening. A second heavily doped layer of polysilicon (80) is provided within the base contact opening, forming a first base contact electrode to the base region of the substrate. A second base contact (66) is formed to the buried layer underlying the emitter and collector regions (76,78). The structure is annealed to diffuse dopant from the emitter and collector electrodes, forming emitter and collector regions in the substrate surface. A **well region** of opposite type extends between them forming the base region. The base contact electrodes are formed by the second polysilicon layer and the underlying part of the heavily doped buried layer respectively.

ADVANTAGE - Allows smaller base width. Increases efficiency. Reduces base contact resistance by using direct polysilicon contact. Increases ft and fmax. Increases current gain by improving emitter efficiency. Allows more flexible contact placement.

Dwg.2/10

L16 ANSWER 7 OF 27 WPIX (C) 2002 THOMSON DERWENT

AN 1996-202296 [21] WPIX

CR 1994-103266 [13]; 2002-207696 [49]; 2002-207697 [49]; 2002-207698 [49]; 2002-228915 [49]; 2002-228916 [49]

DNN N1996-169744

TI **Transistor** mfr. method for bipolar, CMOS and DMOS - by forming MOS **transistor** gate isolated from channel region and adjusting threshold voltage by putting dopants into the channel region with implant energy enough to penetrate gate to implant into channel region.

DC U11 U12 U13

IN CHEN, J W; CORNELL, M E; WILLIAMS, R K; YILMAX, H; CHEN, W; YILMAZ, H

PA (SILI-N) SILICONIX INC

CYC 5

| | | | | | | |
|---|---|---|---|---|---|---|
| PI | EP 708482 | A2 | 19960424 | (199621)* | EN | 70p |
| | R: DE IT NL | | | | | |
| | US 5541123 | A | 19960730 | (199636) | | 67p |
| | US 5541125 | A | 19960730 | (199636) | | 67p |

AB EP 708482 A UPAB: 20020508

The method involves forming a MOS **transistor** gate (351) overlying and isolated (357) from a channel region (360) on an N-type substrate (42). A P-type source region (352) is formed. The **transistor** threshold voltage is adjusted by implanting P+type dopants into the channel region at an implant energy such that the dopants penetrate the gate to implant into the channel region.

The dopants change the threshold voltage. The adjustment is made after forming a diffused body (308) or base region (310) of another **transistor** in the same substrate to prevent the dopants in the channel region from being subjected to diffusion.

USE/ADVANTAGE - Simultaneously forms bipolar **transistors**, high voltage and low voltage CMOS **transistors**, DMOS

**transistors**, zener diodes, and thin film resistors or any desired
combination on same **integrated circuit chip**.
29a,b,c/35

L16 ANSWER 8 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1995-394575 [51] WPIX
DNN N1995-287712 DNC C1995-169881
TI Power **IC** structure - having vertical IGBT and driving and
integrated control structure.
DC L03 U12 U13
IN ZAMBRANO, R
PA (CONS-N) CONSORZIO RICERCA SULLA MICROELETTRONICA
CYC 6
PI EP 683529 A1 19951122 (199551)* EN 14p
R: DE FR GB IT
JP 07321321 A 19951208 (199607) 8p
US 5556792 A 19960917 (199643) 10p
US 5703385 A 19971230 (199807) 10p
ADT EP 683529 A1 EP 1994-830230 19940519; JP 07321321 A JP 1995-117168
19950516; US 5556792 A Div ex US 1995-443908 19950517, US 1995-472196
19950607; US 5703385 A US 1995-443908 19950517
PRAI EP 1994-830230 19940519
AB EP 683529 A UPAB: 19951221
A power **integrated circuit** (PIC) comprises a lightly
doped semiconductor layer (2,2',2'') of first **conductivity-**
**type** superimposed on a heavily doped semiconductor substrate (3)
of second **conductivity-type**, having a vertical
insulated Gate Bipolar **Transistor** (IGBT) and driving and control
circuitry including at least channel MOSFET's of first
**conductivity-type**. The MOSFET's are formed inside
**well regions** (15) of second **conductivity-**
**type** which are included in at least one isolated lightly
**doped region** of first **conductivity-**
**type**, completely surrounded by, and isolated from the lightly
doped layer by means of an isolation region (12,13) of second
**conductivity-type**.
Also claimed is a process for mfg. a PIC structure as above.
USE - Used the in mfr. of **integrated circuits** to
provide a structure with one or more power parts, and driving control and
protection circuitry.
ADVANTAGE - The isolation regions, surrounding the p-type
**well regions**, can have heavier doping compared to the
p-type wells, to reduce the gain of the n-p-n parasitic **transistor**
and thus prevent parasitic SCR latch-up.
Dwg.1/4

L16 ANSWER 9 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1995-394569 [51] WPIX
DNN N1995-287708 DNC C1995-169876
TI Power **IC** structure - in which MOSFET driving and control
circuitry are isolated from the power stage by isolation regions around
the MOSFET wells.
DC L03 U12 U13
IN ZAMBRANO, R
PA (CONS-N) CONSORZIO RICERCA SULLA MICROELETTRONICA
CYC 2
PI EP 683521 A1 19951122 (199551)* EN 13p
JP 07321214 A 19951208 (199607) 9p
US 5591662 A 19970107 (199708) 10p

US 5602416 A 19970211 (199712) 10p
ADT EP 683521 A1 EP 1994-830229 19940519; JP 07321214 A JP 1995-121468 19950519; US 5591662 A Div ex US 1995-443053 19950517, US 1995-471902 19950607; US 5602416 A US 1995-443053 19950517
PRAI EP 1994-830229 19940519
AB EP 683521 A UPAB: 19951221
Power **IC** comprises: heavily doped substrate (3) of first type; lightly doped layer (2) of first type; and integrated first and second type channel MOSFETs formed in first and second type wells (15,14) respectively which are completely isolated from layer two by second type isolation regions (12,13). Pref. region (12) is a buried region and region (13) is a heavily **doped** annular **region**. Structure is formed by: forming buried region (12) in layer (2); forming **well region** (15); simultaneously forming heavily doped deep power stage regions (4) and annular isolation regions (13); adding thin gate oxide (8) and poly gate (19,20) for drive and control circuitry; forming lightly **doped** power stage **regions** (5); forming high dosage **doped** contact **region** for regions (5) as well as source/drain (18) for the first type MOSFETs and contact region (17) to the lightly **doped region**; and forming high dosage source/drain (16) for the second type MOSFETs.

ADVANTAGE - Structure has driving and control circuitry comprising n and p channel MOSFETs fully isolated from the power stage. The power stage can comprise a vertical double-diffused MOSFET or a vertical bipolar junction **transistor**.
Dwg.1/11

L16 ANSWER 10 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1995-240119 [31] WPIX
CR 1994-191543 [23]
DNN N1995-187245 DNC C1995-110144
TI Bipolar **transistor** for silicon **integrated circuits** - comprises self-aligned heavily **doped** collector **region** and base link regions.
DC L03 U11 U12 U13
IN WYLIE, I W
PA (NELE) NORTHERN TELECOM LTD
CYC 1
PI US 5428243 A 19950627 (199531)* 11p
ADT US 5428243 A Div ex US 1993-1706 19930107, US 1993-158544 19931129
FDT US 5428243 A Div ex US 5320972
PRAI US 1993-1706 19930107; US 1993-158544 19931129
AB US 5428243 A UPAB: 19950810
Bipolar **transistor** structure comprises: (a) a substrate (32) with a **well region** of a first **conductivity type** and an underlying heavily doped lined layer (34) of the first **conductivity type**; (b) a base formed in a surface region of the **well region** with a heavily **doped** intrinsic base **region** (52) of a second **conductivity type** and an adjacent extrinsic base region (52) of the second **conductivity type**; (c) a layer of material of the first **conductivity type** defining an emitter structure (58) overlying and self-aligned with the intrinsic base region (50) and forming an emitter-base junction (61); (d) a heavily doped local collector (54) region of the first **conductivity type** provided in the **well region** underlying the intrinsic base region (52) and self-aligned with emitter-base junction, the local collector region (54) contacting the underlying buried layer; (e) dielectric isolation on sidewalls of the emitter structure from the extrinsic base region; (f) the

top of the emitter structure providing a planarised emitter contact area self-aligned within an area defined by the underlying intrinsic base region; and (g) base contacts provided to the extrinsic base region. A single polysilicon bipolar **transistor** is also claimed.

USE - Used in Si **integrated circuits**.

ADVANTAGE - Problems such as the non-planar topography of a thick polysilicon layer are overcome making subsequent steps such as metallisation and dielectric planarisation easier. Also the risk of damage to the emitter-base junction area of the substrate Si during etching is reduced. Base resistance and/or emitter-base edge leakage problems are reduced.

Dwg.8/12

L16 ANSWER 11 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1995-138295 [18] WPIX
DNN N1995-108669 DNC C1995-063992
TI Mfr. of CMOS **transistor** with metal gate - involves using first-type substrate with second-type well to produce first-type MOS **transistor** and second-type **transistor**.
DC L03 U11 U13
IN YANG, S
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 2
PI TW 241383 A 19950221 (199518)* 16p
US 5486482 A 19960123 (199610)# 9p
ADT TW 241383 A TW 1994-109041 19940930; US 5486482 A US 1995-437724 19950509
PRAI TW 1994-109041 19940930; US 1995-437724 19950509
AB TW 241383 A UPAB: 19950518

Prodn. of a CMOS **transistor** with metal gate, which is applicable to the first type substrate with the second type well for producing the first type MOS **transistor** and the second type **transistor**, includes:

(1) forming a shield on the predetermined position of the second type well and the first type substrate to define the shift of the first type and second type MOS **transistor** between the shield;

(2) implementing oxidation by using shield as mask, and forming the first field oxide on the second type well and the first type substrate between shield, removing the first field oxide;

(3) doping separately the first type dopant and the second type dopant to the second type well and the first type substrate by using the shield as mask to form the shift of the first type and second type MOS **transistor**;

(4) implementing oxidn. by using shield as mask to form the second field oxide separately on the shift;

(5) removing the shield;

(6) doping separately the first type dopant and the second type dopant to the second type well and the first type substrate between shift, and forming heavily **doped area** and lightly **doped** are under the heavily **doped area** separately to form the drain and source of the first type and the second type MOS **transistor** separately;

(7) implementing oxidn. to form gate oxide between the drain and source, simultaneously forming isolating oxide with thickness larger than the gate oxide's; and

(8) implementing metallisation to form the metal gate of the first type and the second type MOS **transistor** and the contact metal of above drain and source.

USE - Mfr. of CMOS **transistor** with metal gate with self-alignment.

Dwg.0/6

L16 ANSWER 12 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1995-100719 [14] WPIX
DNN N1995-079659
TI **Integrated circuit** with FET source-drain coupled through resistor to conductor - has resistor formed in **doped** tub **region** connected by heavily doped contact to output conductor, with resistor size defined by masking conductor formed in gate conductor layer.
DC U13
IN SMOOHA, Y
PA (AMTT) AT & T CORP; (AMTT) AMERICAN TELEPHONE & TELEGRAPH CO; (LUCE) LUCENT TECHNOLOGIES INC
CYC 4

| | | | | | |
|---|---|---|---|---|---|
| PI | GB 2281813 | A | 19950315 | (199514)* | 14p |
| | JP 07183516 | A | 19950721 | (199538) | 6p |
| | GB 2281813 | B | 19970416 | (199719) | |
| | US 5838033 | A | 19981117 | (199902) | |
| | KR 204986 | B1 | 19990615 | (200063) | |

ADT GB 2281813 A GB 1994-17498 19940831; JP 07183516 A JP 1994-238605 19940907; GB 2281813 B GB 1994-17498 19940831; US 5838033 A US 1993-118109 19930908; KR 204986 B1 KR 1994-22412 19940907
PRAI US 1993-118109 19930908
AB GB 2281813 A UPAB: 19950412
The **IC** includes a FET with a gate conductor (406) formed from a layer over a semiconductor substrate (400). The resistor is formed in a **well region** (401) connected to a circuit conductor (410) through a heavily **doped** contact **region** (402) in the tub. The tub and contact region are the same **conductivity type** as the FET source-drain region. The FET source-drain region is also connected to the circuit conductor.

The resistor underlies a resistor masking conductor (408) formed from the conductor layer, so that the resistor mask defines the resistor size. Pref. the resistor masking conductor is connected (409) to the circuit conductor, which may be an output conductor connected to a bond pad.

USE/ADVANTAGE - ESD protection; output buffer. Min. lithographic feature size for resistor length; reduced buffer size; avoids extra process steps e.g. for LDD.
Dwg.4/6

L16 ANSWER 13 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1994-103266 [13] WPIX
CR 1996-202296 [21]; 2002-207696 [49]; 2002-207697 [49]; 2002-207698 [49]; 2002-228915 [49]; 2002-228916 [49]
DNN N1994-080633
TI Isolated well structure for **transistor** in BiCDMOS **integrated circuit** process - has vertical **transistor** formed in well at upper surface of epitaxial layer, separated and isolated from substrate layer by buried well in epilayer and buried isolation region in epilayer and substrate.
DC U11 U12 U13
IN CHEN, J W; CORNELL, M E; WILLIAMS, R K; YILMAZ, H; CHEN, W
PA (SILI-N) SILICONIX INC
CYC 6

| | | | | | | |
|---|---|---|---|---|---|---|
| PI | EP 589675 | A2 | 19940330 | (199413)* | EN | 64p |
| | R: DE FR IT NL | | | | | |
| | US 5374569 | A | 19941220 | (199505) | | 56p |
| | JP 07007094 | A | 19950110 | (199511) | | 39p |

US 5416039 A 19950516 (199525) 57p

AB EP 589675 A UPAB: 20020508
The isolated well structure includes an epitaxial layer on a semiconductor substrate layer of opposite conductivity. A buried isolation region extends into the substrate and epitaxial layers, beneath the epilayer upper surface and is of the same **conductivity type** as the substrate. A buried well in the epitaxial layer, and of the same **conductivity type**, extends upward from the buried isolation region upper surface.

A **well region** in the epitaxial layer, of the same conductivity, extends down from the upper surface of the layer. The **well region** lower surface contacts the top of the buried well. The well and buried well are both electrically isolated and separated from the substrate. The **well region** is of the first **conductivity type**. A **transistor** is formed in the well at the upper surface of the epitaxial layer.

USE/ADVANTAGE - Complementary bipolar **transistor** analog circuitry, CMOS **transistors** for high power digital switching and digital logic circuitry, DMOS power **transistors**, buried Zener diodes, thin film resistors, all in single **wafer** or **IC** . Fewer masking steps in mfr.; improved yield.
Dwg.18/26

L16 ANSWER 14 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1992-398286 [48] WPIX
DNN N1992-303863
TI High DC breakdown voltage for **integrated circuit** I-O protection transfer gate - has externally connected source or drain formed in **well region** to reduce electric field gradient at substrate junction.
DC U12 U13
IN CO, R; LIANG, J C; OUYANG, K W
PA (WDIG-N) WESTERN DIGITAL CORP
CYC 1
PI US 5162888 A 19921110 (199248)* 7p
ADT US 5162888 A US 1989-351669 19890512
PRAI US 1989-351669 19890512
AB US 5162888 A UPAB: 19931006
The field effect **transistor** formed in a substrate having a layer of a semiconductor material of a first **conductivity type** comprises a **well region** of a second **conductivity type** semiconductor material formed in the upper surface of the substrate having a doping concentration of approximately 10 power 15 dopant atoms/cc and extending into said substrate to a depth of approximately 4 microns or greater. A first highly **doped region** of the second **conductivity type** semiconductor material is formed within the **well region**. A second highly **doped region** of second **conductivity type** semiconductor material is formed in the substrate upper surface at a position spaced apart from the first highly **doped** and **well regions**.

The spaced apart first and second highly **doped regions** define a channel region. A gate oxide layer is formed over the channel region having a maximum thickness of approximately 100-1000 Angstroms. A gate electrode is formed on the gate oxide with first contact electrodes formed on the highly **doped regions**. The **well region** has a depth into the upper substrate surface of 2-20 times that of the first highly **doped region**.

USE/ADVANTAGE - Withstands connection to DC voltages larger than on-**chip** supply. Compatible with current VLSI processing.
1/2

L16 ANSWER 15 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1991-376669 [51] WPIX
DNN N1991-288293
TI High voltage lateral **transistor** for **integrated circuit** - has buried base formed of **well region** and oppositely **doped well region** formed surrounding collector region in lateral PNP **transistor**.
DC U11 U12
IN SCOTT, D B; TRAN, H V
PA (TEXI) TEXAS INSTR INC
CYC 2
PI US 5070381 A 19911203 (199151)*
JP 04221835 A 19920812 (199239) 12p
ADT US 5070381 A US 1990-496487 19900320; JP 04221835 A JP 1991-56908 19910320
PRAI US 1990-496487 19900320
AB US 5070381 A UPAB: 19930928
The invention provides a structure and method for incorporating a high voltage lateral bipolar **transistor** in an **integrated circuit**.

A buried base contact is formed and the base itself is formed of a wall region in the **integrated circuit**. An oppositely **doped well region** is formed surrounding the collector region in the lateral PNP **transistor**. This collector well is formed of the opposite **conductivity type** of the base well. Contact to the collector and a heavily doped emitter are then formed in the collector well and base well respectively.

The more lightly doped collector well provides a thick depletion region between the collector and base and thus provides higher voltage operation. The positioning of the base/collector junction to the collector well at base well junction also reduces the spacing between the collector and the emitter.

ADVANTAGE - This reduced spacing provides greater carrier injection from the forward biased base/emitter junction to the reverse biased base/collector junction. Thus, the performance of the lateral PNP **transistor** is improved. This structure is easily incorporated with standard BiCMOS processing and may be incorporated with other bipolar processing.
15/15

L16 ANSWER 16 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1991-304688 [42] WPIX
DNN N1991-233434 DNC C1991-131900
TI BICMOS **integrated circuit** with self-aligned well tap - to provide improved packing density and lower layer-to-substrate capacitance.
DC L03 U11 U13
IN ILDEREM, V; LEIBIGER, S M
PA (NASC) NAT SEMICONDUCTOR CORP
CYC 7
PI EP 451632 A 19911016 (199142)*
R: DE FR GB IT
US 5079182 A 19920107 (199205)
JP 06045532 A 19940218 (199412) 14p
EP 451632 A3 19940706 (199528)
US 5466960 A 19951114 (199551) 16p

KR 230610 B1 19991115 (200111)
ADT EP 451632 A EP 1991-104941 19910328; US 5079182 A US 1990-503345 19900402; JP 06045532 A JP 1991-144279 19910402; EP 451632 A3 EP 1991-104941 19910328; US 5466960 A Div ex US 1990-503345 19900402, US 1991-753272 19910820; KR 230610 B1 KR 1991-4978 19910329
FDT US 5466960 A Div ex US 5079182
PRAI US 1990-503345 19900402; US 1991-753272 19910820
AB EP 451632 A UPAB: 19930928
A substrate (10, 11) has a channel region (20e) of first **conductivity type** and source (20a) and drain (20b) regions, formed in a **doped well region** (12) of first **conductivity type**. The channel (20c) is separated from a doped poly-Si gate (30) by an oxide layer (38). The source, gate and drain define a first field effect device (4). At least one of the source and drain regions is overlain by a first **doped** poly-Si **region** of first **conductivity type**. A method is claimed for forming a combination well top (32) and source/drain contact (28) for the field effect device, comprising: (a) forming a connective region of first **conductivity type** in the substate adjacent to one of the source or drain regions and a portion of the first poly-Si region to provide a conductive path between the **well region** and the first **doped** poly-Si **region** to configure first poly-Si region as a well tap (32); and (b) forming metal silicide (54a, b) on upper surface and sidewall surface of the first polysilicon region and part of the upper surface of source and/or drain to form a conductive path between source or drain to the said first poly-Si region which is thereby configured as a contact for the source or drain so connected.
USE/ADVANTAGE - Used for **integrated circuits** of BiCMOS type which combine high packing density and low power consumption of CMOS device with the high speed of bipolar devices A self-aligned well tap formed using single poly-Si and silicide technologies avoids the need for a well tap laterally spaced from source and drain regions. This allows a redn. is space used and therefore an increase in packing density. @(20pp Dwg.No.1/4)@

L16 ANSWER 17 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1991-216665 [30] WPIX
DNN N1991-165328 DNC C1991-094043
TI Self aligned power DMOS cell with resistance to sec. breakdown - comprising semiconductor layer contg. D-**well region** with gate over region, and source region and first protection region in layer.
DC L03 U12 U13
IN COTTON, D R; EFLAND, T R; JONES, R C; LEE, J K; TODD, J R; BLANTON, C H; LATHAM, L; MOSHER, D M; TODD, B; TROGOLO, J R
PA (TEXI) TEXAS INSTR INC
CYC 7
PI EP 437939 A 19910724 (199130)*
R: DE FR GB IT NL
US 5119162 A 19920602 (199225) 24p
US 5181095 A 19930119 (199306) 25p
US 5256582 A 19931026 (199344)#
JP 06318707 A 19941115 (199505) 19p
ADT EP 437939 A EP 1990-313365 19901210; US 5119162 A CIP of US 1989-309515 19890210, US 1989-454811 19891219; US 5181095 A Cont of US 1989-309515 19890210, Cont of US 1990-561490 19900801, Div ex US 1991-671625 19910319, US 1991-688196 19910419; US 5256582 A Cont of US 1989-309515 19890210, Cont of US 1990-561490 19900801, Cont of US 1991-671625 19910319, US

1991-800869 19911127; JP 06318707 A JP 1990-419274 19901219
PRAI US 1989-454811 19891219
AB EP 437939 A UPAB: 19930928
A DMOS structure comprises a layer of semiconductor material of a first doping type, forming drift and drain regions; a D-**well region** in the layer, of a second doping type opposite the first; a gate over the D-**well region**; a source region in the layer, of a first doping type; a first protection in the layer, of a second doping type and coupled to the gate.

The first protection region is located so that the breakdown voltage of the diode formed by the first protection region with the drift and drain regions is less than the breakdown voltage of the diodes formed by the D-well with the drift and drain regions.

Pref. the structure further comprises: in the D-**well region** a lightly **doped** channel **region** adjacent the gate, and a heavily **doped** second protection **region** located at areas of high electric field during breakdown of the diode formed by the D-well with the drift and drain regions.

USE/ADVANTAGE - Self-aligned Power DMOS cell, which improves the ruggedness of the device making it less susceptible to sec. breakdown, and improves the SOA of the device under both reverse and forward bias safe operating conditions experienced when driving inductive or commutating loads.
1/6

L16 ANSWER 18 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1989-085034 [11] WPIX
DNN N1989-064890 DNC C1989-037795
TI Bulge well trench device in **IC** - mfd. by forming doped epitaxial layer on substrate, forming doped well of opposite type and forming trenches and isolation region.
DC L03 U11 U12
IN BARDEN, J M; PARRILLO, L C
PA (MOTI) MOTOROLA INC
CYC 1
PI US 4808543 A 19890228 (198911)* 7p
ADT US 4808543 A US 1986-860734 19860507
PRAI US 1986-860734 19860507
AB US 4808543 A UPAB: 19930923
A method for making an **IC** comprises forming at least one doped well (38,40) in a semiconductor substrate (22), with several trenches (32) being formed in the well using a mask, and forming at least one similarly **doped region** at the bottom of the trenches (34) and extending below the bottom of the doped well, by doping the impurity solely into the bottom of the trenches (34) using the same mask, and then driving the dopant to expand the bottom (36) of the **doped well regions**.

Also claimed is a method as above in which at least one **doped well region** is of opposite **conductivity type** and which ends by forming an isolation region (48).

Further claimed is a method of making a bulge well structure similar to the above which forms a doped epitaxial layer on the substrate before forming at least one doped well of opposite type in this layer, then forming the trenches above and an isolation region.

USE/ADVANTAGE - **ICs** with trench devices such as capacitors for DRAMs and **transistors** which have better soft error protection and lower junction leakage are provided. Heavily doped or very deep wells are not needed in providing trench devices in a well of opposite **conductivity type** to the substrate, nor are

extra masking steps.
8/8

L16 ANSWER 19 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1987-272653 [39] WPIX
DNN N1987-204202 DNC C1987-115750
TI Doped well prodn., in **integrated circuit** - contg.
bipolar **transistor**, involving partial compensation of dopants.
DC L03 U11 U12
IN HUNT, R G
PA (STTE) STC PLC
CYC 10
PI EP 239217 A 19870930 (198739)* EN 12p
R: BE CH DE FR GB IT LI NL
GB 2188478 A 19870930 (198739)
JP 62235781 A 19871015 (198747)
GB 2212327 A 19890719 (198929)
GB 2188478 B 19891122 (198947)
GB 2212327 B 19891206 (198949)
US 4873199 A 19891010 (198950) 7p
EP 239217 B 19901128 (199048)
R: BE CH DE FR IT LI NL
DE 3766397 G 19910110 (199103)
ADT EP 239217 A EP 1987-301239 19870213; GB 2188478 A GB 1989-5393 19890309;
JP 62235781 A JP 1987-71297 19870325; GB 2212327 A GB 1986-7593 19860326;
GB 2188478 B GB 1986-5393 19860326; US 4873199 A US 1988-249205 19880923
PRAI GB 1986-7593 19860326; GB 1989-5393 19890309
AB EP 239217 A UPAB: 19930922
(A) A doped well is formed in a major surface of semiconduc-tor substrate by introducing a first dopant into the **well region** and introducing a second dopant of opposite **conductivity type** into the surface of the **well region**, partial compensation of the dopants being effected such that the net max. concn. is disposed below the surface.

(B) A doped well is formed in a major surface of a silicon substrate by implanting P ions into the substrate in the wall region, heating the substrate to drive in the implant, implanting B ions into the **well region** and heating the substrate to drive in the B ion implant, the relative implanted doses of the two ions being such that partial compensation of the dopants is effected within the **well region**.

(C) Also claimed is mfr. of a bipolar polysilicon emitter **transistor**.

USE/ADVANTAGE - The processes are used to form doped wells in **ICs** including bipolar devices. By providing compensation of the dopants, the breakdown voltage of a bipolar **transistor** formed in the well is maintained while the collector resistance is insignificantly reduced.
10/10

L16 ANSWER 20 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1985-106407 [18] WPIX
DNN N1985-079766 DNC C1985-046118
TI **IC** contg. FET and bipolar **transistor** - has collector
electrode and gate electrode formed from single high impurity concn.
layer.
DC L03 U11 U13
IN IWASAKI, H
PA (TOKE) TOSHIBA KK

CYC 5
PI EP 139266 A 19850502 (198518)* EN 19p
R: DE FR GB
JP 60080267 A 19850508 (198525)
EP 139266 B 19890125 (198904) EN
R: DE FR GB
DE 3476493 G 19890302 (198910)
US 4818720 A 19890404 (198916)
US 4965220 A 19901023 (199045)
JP 03015346 B 19910228 (199113)
ADT EP 139266 A EP 1984-111849 19841003; JP 60080267 A JP 1983-187930 19831007; US 4818720 A US 1987-96241 19870908; US 4965220 A US 1989-306393 19890206; JP 03015346 B JP 1983-187930 19831007
PRAI JP 1983-187930 19831007
AB EP 139266 A UPAB: 19930925
An **IC** comprises a bipolar **transistor** and FET, where the gate electrode (38,39) of the FET and collector electrode (372) of the bipolar **transistor** are formed from a common electrode layer (102) of high impurity concn. The collector region includes a region of high impurity concn. of the same **conductivity type** as the collector.

The **IC** is mfd. by (a) forming first region (241,242) of high conc. second type impurity in a first type semiconductor substrate (23); (b) forming a second epitaxial layer region (25) of first **conductivity type** on the substrate; (c) forming a third, second type region(s) (261,262) in the second region, electrically connected to the first region(s); (d) forming an FET in the second or third region, including forming gate electrodes (38,39) for the FET and simultaneously forming collector and emitter electrodes (371,372) of the bipolar **transistor**; (e) forming a bipolar **transistor** in the third region; and (f) forming a fourth, deep, high impurity concn. second type region (100) in the third region using the collector electrode as impurity source.

ADVANTAGE - The FET is operable at high speed, and the bipolar **transistor** has high cut off frequency, low ON-resistance, low power consumption, and pref. suppressed latch up.
2G/3

L16 ANSWER 21 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1985-020882 [04] WPIX
DNN N1985-015260
TI **Integrated circuit** overload protection device - has collector of protecting **transistor** connected to power supply terminal which is opposed to terminal coupled to protected **transistor**.
DC U13 U24
IN HARFORD, J R
PA (RADC) RCA CORP
CYC 1
PI GB 2142778 A 19850123 (198504)* 5p
GB 2142778 B 19850724 (198530)
ADT GB 2142778 A GB 1984-19706 19830629; GB 2142778 B GB 1982-19706 19820607
PRAI US 1981-273325 19810615
AB GB 2142778 A UPAB: 19930925
A bipolar **transistor** of opposite type to a protected amplifying **transistor** (Q1) is connected with its base to the collector of the amplifying **transistor** (Q1) Its collector is connected to the terminal of the power supply which is not connected to a terminal (+V) of the load resistor (Rl) of the protected **transistor**.

The emitter of the protecting **transistor** (Q2) is pref. connected to the base of the protected **transistor** (Q1) through a protective resistor (Rp). Input to the protected **transistor** (Q1) are provided at the interconnection of the emitter of the protecting **transistor** (Q2) with one terminal of the protective resistor (Rp).

USE - For preventing negative feedback amplifier from becoming a positive feedback amplifier.

2/4

L16 ANSWER 22 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1984-070721 [12] WPIX
DNN N1984-053371
TI Bipolar and CMOS **transistor integrated circuit** mfr. - provides isolation, low threshold voltage, high breakdown voltage, and avoids parasitic components.
DC U11 U13
IN ANZAI, N; MURAMATSU, A; TANIZAKI, Y; YASUOKA, H
PA (HITA) HITACHI LTD
CYC 8

| | | | | | |
|---|---|---|---|---|---|
| PI | FR 2531812 | A | 19840217 | (198412)* | 27p |
| | DE 3329224 | A | 19840315 | (198412) | |
| | GB 2126782 | A | 19840328 | (198413) | |
| | JP 59031052 | A | 19840218 | (198413) | |
| | GB 2126782 | B | 19860625 | (198626) | |
| | US 4662057 | A | 19870505 | (198720) | |
| | IT 1163907 | B | 19870408 | (198928) | |
| | DE 3329224 | C2 | 19931202 | (199348) | 10p |

ADT FR 2531812 A FR 1983-13245 19830812; DE 3329224 A DE 1983-3329224 19830812; GB 2126782 A GB 1983-21642 19830811; JP 59031052 A JP 1982-139932 19820813; US 4662057 A US 1985-759441 19850725; DE 3329224 C2 DE 1983-3329224 19830812
PRAI JP 1982-139932 19820813
AB FR 2531812 A UPAB: 19930925

The semiconductor has an epitaxial layer of low conductivity so that it is possible to attain a low threshold voltage of the p-type MOST and a high breakdown voltage of the npn **transistor**. Similarly, the conductivity of a p-well is low and precise so that it is possible to attain a low voltage of the n-type MOST.

A thick oxide layer prevents lateral diffusion as layers are formed, increasing isolation between the npn **transistor** region and the CMOS region, between two CMOS **transistors** and between the base and the collector conductor of the npn **transistor**. This allows greater density of integration. The polysilicon gates provide alignment masks for the formation of the drain and source of each MOST providing a gate length of 5 microns. Ion-implanted channel stops prevent the formation of parasitic MOSTs and a buried n+ layer prevents the formation of a parasitic thyristor in the CMOS region by providing a high conductivity path at the lower edge of the epitaxial layer . One stage of mfr. combines formation of well and isolator and another stage combines formation of n-channel drain, source and emitter with addition of ions to collector connector .

0/13

L16 ANSWER 23 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1982-16005E [09] WPIX
TI Semiconductor device esp. integrated injection **logic circuit** - with insulating layer preventing collector base short circuit.
DC L03 U13

IN SHINOZAKI, S
PA (TOKE) TOKYO SHIBAURA ELECTRIC CO
CYC 2
PI DE 3129755 A 19820225 (198209)* 23p
JP 57028352 A 19820216 (198212)
DE 3129755 C 19860306 (198611)
ADT DE 3129755 A DE 1981-3129755 19810728
PRAI JP 1980-103340 19800728
AB DE 3129755 A UPAB: 19930915
Semiconductor device consists of a dielectric isolated semiconductor island zone (I) of a first **conductivity type**, a first and a second **well region**, (II) and (III) respectively, formed in (I), which are of the opposite **conductivity type** and form a lateral **transistor**, semiconductor zone(s) (IV) of the first **conductivity type** formed in (II), which form a vertical **transistor** with (II) and (I), and a polycrystalline Si layer (V), which covers the semiconductor **zone** and is **doped** with an impurity of the first **conductivity type**. The novel feature is that there is a first insulating layer (VI) surrounding the semiconductor zones between (V) and (II), which covers at least one junction between the semiconductor zones and (II) and extends over (II).

The device pref. is an **IC** of the I2L type. With (VI) in the structure, the collector-base junction is not exposed during etching to form the base contact window, preventing collector-base short circuit on metallisation. Also, the collection of minority charge-carriers in base or emitter zones of the reversed npn-**transistor** can hardly increase, whilst the operating speed is higher than usual and a satisfactory great integration density can be produced.

L16 ANSWER 24 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1998-050859 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR **INTEGRATED CIRCUIT**
IN MIYAWAKI YOSHIHIKO; MORIKAWA NARIHIRO
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
PI JP 10050859 A 19980220 Heisei
AI JP1996-199293 (JP08199293 Heisei) 19960729
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 2
AB PURPOSE: TO BE SOLVED:To provide the manufacture method of a semiconductor device which can considerably reduce influence on the other element at the time of incorporating a high withstand voltage-type element in a **well area** whose **conduction type** is opposite to that of a substrate.
CONSTITUTION: he time of forming the N-type **well area** 13 in the P substrate 11, the half of the **well area** 13 is diffused by heat treatment for the first time and impurities forming the lightly **doped** drain **area** 15 of high withstand voltage MOS are ion-implanted. Then, the N-type **well area** 13 is diffused and the lightly **doped** drain **area** 15 is diffused by heat treatment for the second time. Then, a channel stopper area 18, a LOCOS oxidized film and respective MOS **transistors** are formed. Since the lightly **doped** drain **area** 15 is diffused by using a part of the heat diffusion treatment of the N-type **well area** 13, heat history is prevented from being excessively increased.

L16 ANSWER 25 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1995-147326 JAPIO

TI MANUFACTURE OF SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN YAMAOKA TORU
PA MATSUSHITA ELECTRON CORP, JP (CO 000584)
PI JP 07147326 A 19950606 Heisei
AI JP1993-295146 (JP05295146 Heisei) 19931125
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 6
AB PURPOSE: To make a semiconductor element fine while its reliability and its withstand voltage are being ensured.
CONSTITUTION: A thin silicon oxide film is grown on a P-type silicon substrate 1 on which an N-**well region** 5 and a P-**well region** 6 have been formed, and a silicon nitride film is formed selectively on a region on the N-**well region** 5 of the silicon oxide film. Then, a field doping and implantation operation and an anti-punchthrough doping and implantation operation are executed continuously to the P-**well region** 6 at different acceleration energies, and an anti- punchthrough **doped region** 9 and a field **doped region** 12 are formed, and a thick silicon oxide film 11 is grown selectively. Thereby, an extreme drop in the surface concentration of a field region is suppressed, and a sufficient process margin can be ensured with reference to the drain withstand voltage of a field- effect **transistor** of a second **conductivity type** and to a field inversion voltage in a **well region** of a first **conductivity type**.

L16 ANSWER 26 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1988-002370 JAPIO
TI SEMICONDUCTOR DEVICE
IN YAO TAKEYUKI; MIHARA TERUYOSHI
PA NISSAN MOTOR CO LTD, JP (CO 000399)
PI JP 63002370 A 19880107 Showa
AI JP1986-144740 (JP61144740 Showa) 19860623
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 620, Vol. 12, No. 2, P. 36 (19880611)
AB PURPOSE: To inhibit the operation of a parasitic **transistor** without increasing the area of a **chip** by forming a polycrystalline silicon region having the same **conductivity type** as a substrate region and high impurity concentration in size deeper than a source region and a drain region and bringing the polycrystalline silicon region to the same potential as the source region.
CONSTITUTION: Polycrystalline silicon regions 26, 27 are each shaped at a position in the vicinity of the side of an n+ source region 3 in an nMOS 8 and at a position in the vicinity of a borderline region with a pMOS 17 in size deeper than the n+ source region 3 and an n+ drain region 4 in a p **well region** 2. An impurity having the same **conductivity type** as the p **well region** (a substrate **region**) 2 is **doped** to the polycrystalline silicon regions 26, 27 in high concentration, land the regions 26, 27 are brought to a p+ type. An impurity having the same **conductivity type** as an n-type substrate **region** 1 is **doped** to polycrystalline silicon regions 28, 29 in high concentration, and the regions 28, 29 are brought to an n+ type. The polycrystalline silicon region 28 shaped near the side of a p+ source region 12 is connected in common with said p+ source region 12, and supply voltage Vdd is applied to the region 12.

L16 ANSWER 27 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1987-281463 JAPIO

TI MANUFACTURE OF **INTEGRATED CIRCUIT** DEVICE
IN HOTTA MASAHIKO
PA YAMAHA CORP, JP (CO 000407)
PI JP 62281463 A 19871207 Showa
AI JP1986-124950 (JP61124950 Showa) 19860530
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 612, Vol. 12, No. 174, P. 37 (19880524)
AB PURPOSE: To prevent a punch-through without augmenting the number of processes by forming an impurity **doping region** functioning as the increase of the threshold voltage of a field **transistor** and the prevention of the punch- through in combination before field oxidation.
CONSTITUTION: An impurity determining a predetermined **conductivity type** is doped simultaneously to a section to be oxidized in a semiconductor substrate 60 and a prescribed section, to which an FET is shaped, before forming a field insulating film 74 through selective oxidation, thus forming an impurity **doping region** 68 for augmenting imputity concentration just under the field insulating film 74 and preventing a punch-through between a source and a drain in a **transistor**. A P-type **well region** 62 is shaped to the surface of the substrate such as an N-type Si substrate 10, the surface of the substrate is thermally oxidized to form an oxide film 64, a resist layer 66 is shaped, and phosphorus ions are implanted to form a phosphorus-ion implanting region 68. Nitrides are deposited, resist layers 72A and 72B are shaped onto the nitrides, nitride films 70A and 70B are left just under the resist layers 72A and 72B, and the surfaces of the substrate are oxidized selectively to form the field insulating films 74.

L19 ANSWER 1 OF 4 JAPIO COPYRIGHT 2002 JPO
AN 1998-012627 JAPIO
TI SEMICONDUCTOR DEVICE
IN SHIMOIDA YOSHIO; KANEKO HIROYUKI
PA NISSAN MOTOR CO LTD, JP (CO 000399)
PI JP 10012627 A 19980116 Heisei
AI JP1996-178529 (JP08178529 Heisei) 19960619
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 1
AB PURPOSE: TO BE SOLVED:To set a bias point of a collector current in a low current region in all temperature ranges.
CONSTITUTION: rst P+ type emitter diffusion region 7 is surrounded by a second P+ type emitter diffusion region 8, and the first and the second P+ type emitter diffusion regions 7, 8 are surrounded by a P+ type collector diffusion region 5. An N type **well region** 3 is formed so as to cover the entire device, and a base current is controlled with an N type base **contact diffusion** region 4. N and P type MOS **transistors** 15, 16 are switched with a signal from a temperature detector part 11, and a first and a second emitter electrode terminals 12, 17 are connected upon room temperature. Upon high temperature the second emitter electrode terminal 17 and a substrate contact region 18 are connected, and the second P+ type emitter diffusion region 8 is kept at the same electric potential of the substrate 1 to reduce a current amplification rate. Hereby, a dispersion point of the collector current is moved to a low current side, and hence a collector current bias point can be set to the same point as upon the room temperature.

L19 ANSWER 2 OF 4 JAPIO COPYRIGHT 2002 JPO
AN 1989-243472 JAPIO
TI SEMICONDUCTOR DEVICE
IN YOU SEIHATSU; TANIDA YUJI
PA FUJI XEROX CO LTD, JP (CO 359761)
PI JP 01243472 A 19890928 Heisei
AI JP1988-70724 (JP63070724 Heisei) 19880324
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 864, Vol. 13, No. 578, P. 132 (19891220)
AB PURPOSE: To prevent a parasitic bipolar **transistor** effect by forming, adjacent to a source region, a high impurity-concentration layer for forming a well contact having a conductivity type opposite to that of the source region.
CONSTITUTION: A P+ type well **contact diffusion** layer 9 is formed adjoined to an N+ type source region 3 while a diffusion layer 10 having impurity concentration slightly higher than a P-type **well region** and lower than the impurity concentration of the P+ type well **contact diffusion** layer 9 is shaped on at least the source region side to a shape that these region 3 and layer 9 are included. Consequently, the N+ type source region 3 and the P+ type well **contact diffusion** layer 9 are constituted adjacently, and a common electrode is formed, thus bringing both region 3 and layer 9 to the same potential (ground potential) at all times. Since the P-type diffusion layer 10 is formed so as to surround both region 3 and layer 9, a distance contributing to the resistance (Rwell) of the **well region** of ON currents (hole currents) of a parasitic bipolar **transistor** is shortened while the conductivity of the P-type diffusion layer 10 is increased. Accordingly, a parasitic bipolar **transistor** effect is prevented.

L19 ANSWER 3 OF 4 JAPIO COPYRIGHT 2002 JPO
AN 1989-155662 JAPIO
TI SEMICONDUCTOR DEVICE
IN OTOWA YUTAKA; KAWANO KENZO; KO KOICHIRO; KIDA YOSHIHIRO
PA SHARP CORP, JP (CO 000504)
PI JP 01155662 A 19890619 Heisei
AI JP1987-314952 (JP62314952 Heisei) 19871211
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 821, Vol. 13, No. 416, P. 153 (19890914)
AB PURPOSE: To use a p-n junction between a drain region and an opposite conductivity type impurity region as a zener diode by a method wherein an impurity region reverse in conductivity type to a drain is built in a region adjacent to a MOS **transistor** drain region.
CONSTITUTION: On a p-type silicon (100) substrate 8, an n-type epitaxial layer is grown. A p+-type diffusion layer 9 is formed, dividing the n-type epitaxial layer into n-type islands 10. A p- **well region** 11 is formed, and then a CMOS **transistor** section, a gate insulating film 12, and a gate electrode 13 are formed simultaneously. A p-type impurity is diffused for the formation of a substrate **contact diffusion** region 14 and a diffusion region 15. Next, an n-type impurity is diffused for the formation of an anode (source) region 16 and a cathode (drain) region 17. Finally, an insulating film 18 is formed to cover the whole surface of the substrate 8, electrode leadout openings are provided, and a cathode electrode 19 and an anode electrode 20 are formed.

L19 ANSWER 4 OF 4 JAPIO COPYRIGHT 2002 JPO
AN 1986-174672 JAPIO
TI VMOS **TRANSISTOR**
IN MURAKAMI KOICHI
PA NISSAN MOTOR CO LTD, JP (CO 000399)
PI JP 61174672 A 19860806 Showa
AI JP1985-13440 (JP60013440 Showa) 19850129
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 466, Vol. 1, No. 384, P. 85 (19861223)
AB PURPOSE: To prevent the dielectric breakdown of the gate oxide film in the case where a high voltage is impressed on the gate electrode, by providing a second conduction- type **well region** connected to the source region and the first conduction-type high concentration impurity region on a semiconductor substrate.
CONSTITUTION: When a comparatively low, normal, positive voltage is impressed to the gate electrode 17 of a VMOS **transistor** section 23, a conduction channel is induced between the source region 11 and the drain region 3 in the P-type **well region** 9 just under the gate oxide film 15, and is actuated to control the current between the source and the drain. When the gate input voltage is a voltage, such as surge voltage, higher than the Zener voltage of the P-N juctionin the Zener diode section 25, the P-N junction breaks down and becomes conducting. Accordingly, the high surge voltage impressed on the gate electrode 17 is shorted from the electrode 17 not to the gate oxide film 15 but to the sourceelectrode 19 by way of the wiring 31, the high concentration N-type diffusion region 29, the second P-type **well region** 27, the second P-type well **contact diffusion** region 33 and the wiring 33. With this structure, the dielectric breakdown of the gate oxide film 15 due to the application of a high voltage such as of a surge can be prevented.

L23 ANSWER 1 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 2002-081831 [11] WPIX
CR 2000-601130 [41]
DNN N2002-060908 DNC C2002-024622
TI Building of sensor array by forming gate islands spaced closed to each other to prevent formation of **transistor** at each island, and forming p-n junction of photodiode between two regions.
DC L03 U11 U12 U13
IN BREISCH, J E; KANG, J S
PA (ITLC) INTEL CORP
CYC 1
PI US 6306679 B1 20011023 (200211)* 12p
ADT US 6306679 B1 Div ex US 1999-323748 19990601, US 2000-565913 20000505
FDT US 6306679 B1 Div ex US 6091093
PRAI US 1999-323748 19990601; US 2000-565913 20000505
AB US 6306679 B UPAB: 20020215

NOVELTY - A sensor array is built by forming gate islands spaced closed to each other to prevent formation of a **transistor** at each island; forming a p-n junction of a photodiode between first and second regions; and exposing an insulating layer and allowing incident light to pass through the insulating layer and to reach a photosensitive region of the photodiode in the first region.

DETAILED DESCRIPTION - Building of a sensor array includes

(a) placing a first semiconductor layer above a first region (109) of semiconductor material;

(b) patterning the first semiconductor layer as part of a gate formation step in a metal-oxide-semiconductor (MOS) fabrication process used to form field effect **transistor** gates, to yield gate islands (102) that are spaced close to each other to prevent the formation of a **transistor** at each gate island;

(c) forming a second region (113) of semiconductor material in the first region as part of a source/drain formation step in the MOS process;

(d) placing an insulating layer over the first semiconductor layer and the second region;

(e) removing a portion of the insulating layer to expose the first semiconductor layer;

(f) placing a conducting layer over the first semiconductor layer and the insulating layer; and

(g) removing a portion of the conducting layer to expose the insulating layer and allow incident light to pass through the insulating layer and reach a photosensitive region of the photodiode in the first region. The first region has a first **conductivity type**. The second region has a second **conductivity type**. A p-n junction of a photodiode is formed between the first and second regions.

USE - For building a sensor array.

ADVANTAGE - The method avoids the additional mask step typically used to prevent the formation of silicide above the photosensitive regions of the semiconductor that constitutes the photodiodes. The photodiodes exhibit good quantum efficiency and low leakage noise, thus allowing the manufacture of a competitive image sensor **integrated circuit**.

DESCRIPTION OF DRAWING(S) - The figure shows a view of a semiconductor structure obtained when gate islands are spaced wider than twice spacer width.

Gate islands 102
First region 109
Second region 113

Silicide 119, 320
Dwg.3/8

L23 ANSWER 2 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1989-237194 [33] WPIX
CR 1989-196005 [27]; 1989-196013 [27]; 1989-196014 [27]; 1989-224805 [31]; 1990-047953 [07]
DNN N1990-064576 DNC C1990-036736
TI Method of fabricating semiconductor **integrated circuit** - providing accurate control of current amplification factor.
DC L03 U11 U12 U13
IN HAYASAKA, K; HUZINUMA, K; IDOH, N; KUBODA, D; SEKIKAWA, S; TAKETA, K
PA (SAOL) SANYO ELECTRIC CO
CYC 3
PI JP 01171263 A 19890706 (198933)* 5p
US 4898837 A 19900206 (199012)
KR 9204174 B1 19920530 (199349)
ADT JP 01171263 A JP 1987-331176 19871225; US 4898837 A US 1988-271748 19881115; KR 9204174 B1 KR 1988-15291 19881119
PRAI JP 1987-292415 19871119; JP 1987-292416 19871119; JP 1987-292420 19871119; JP 1987-320227 19871217; JP 1987-331176 19871225; JP 1987-320337 19871217
AB JP 01171263 A UPAB: 19940126
A method of fabricating a semiconductor **integrated circuit** comprises the steps of; 1) preparing a semiconductor substrate of a first **conductivity type**, 2) forming buried layers of a second **conductivity type** in regions of the substrate, 3) forming an **epitaxial layer** of the second **conductivity type**, covering the substrate and buried layers, 4) forming isolation regions of the first **conductivity type**, dividing the **epitaxial layer** into islands, 5) selectively implanting ions to form a base region of the first **conductivity type** of a vertical, bipolar **transistor** in a surface layer of one island, and to form a resistor region in a surface layer of another island, this step including a first and a second **ion-implantation**, 6) determining the impurity concn. of the resistor **region** by selectively **doping** impurities into the resistor region and the base region of the vertical, bipolar **transistor**, during the first **ion-implantation**, 7) determining the impurity concn. in the base **region** by selectively **doping** impurities into the base region during the second **ion-implantation**, 8) causing the above a impurities to diffuse to a predetermined depth in the base region, and 9) selectively difusing impurities into a surface layer of the base region, to form an emitter region of the vertical bipolar **transistor**.

USE/ADVANTAGE - The method is used to form a se semiconductor **integrated circuit** which includes a bipolar **transistor** and a reistor, and provides accurate control of the current amplification factor of the **transistor**. (First major country equivalent to J01171263-A)
Dwg.2H/6

L23 ANSWER 3 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1981-32357D [18] WPIX
TI Vertical bipolar **transistor** mfr. - with fewer process steps and **ion implantation** for pref. all doping.
DC L03 U11 U12
IN HUNT, M; KUMAR, R

PA (BURS) BURROUGHS CORP
CYC 1
PI US 4261763 A 19810414 (198118)*
PRAI US 1978-931627 19780807; US 1979-80618 19791001
AB US 4261763 A UPAB: 19930915
The **transistor** is formed in a first **conductivity type** substrate by (a) implanting a substrate region with second-type ats., forming a collector, (b) growing a second type **epitaxial layer** on the surface, covering the collector, (c) implanting a **doped** channel stop **region** in substrate and layer, surrounding and terminating in the collector and (d) growing a field oxide region in the layer, contacting and extending above the channel stop region.

Then, (e) forming a mask for the **transistor** base, with an oversized opening uniformly exposing the entire perimeter of the field oxide, (f) implanting first type ats. to a uniform depth through the opening and oxide perimeter, forming a base terminating throughout its width in the field oxide and (g) forming a base contact and an emitter region extending from portions of the field oxide into the base.

An **IC** contg. high performance, high density devices with high yield potential is formed with fewer fabrication and handling steps than conventional, pref. using only **ion implantation** for doping.

L23 ANSWER 4 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1979-44330B [24] WPIX
TI **Integrated circuit** esp. for integrated injection logic - with inversely driven and complementary vertical and lateral bipolar **transistors**.
DC L03 U11 U12 U13
IN BERGERON, D L; PUTNEY, Z C; STEPHENS, G B
PA (IBMC) IBM CORP
CYC 5
PI EP 2191 A 19790613 (197924)* DE
R: DE FR GB
EP 2191 B 19811104 (198146) DE
R: DE FR GB
DE 2861291 G 19820114 (198203)
CA 1116309 A 19820112 (198206)
IT 1160056 B 19870304 (198918)
PRAI US 1977-855869 19771130; US 1979-69645 19790827
AB EP 2191 A UPAB: 19930901
On a substrate is formed an **epitaxial layer** (1) of one **conductivity type** (a) contg. an embedded, highly **doped zone** (2) of type (a), and embedded zones (3) of opposite conductivity (b).

**Ion implantation** is used to form another embedded zone (4), of type (b), with a concn. profile such that the max. concn. in the intrinsic base regions is displaced so it is nearer zone (2) than the max. concn. in the extrinsic base regions.

In the pref. device, zone (2) in an emitter; and the surface of layer (1) contains a base zone of type (b), the surface of the latter contg. a collector zone of type (a); the result in an I2L structure with complementary vertical and lateral **transistors**.

The charge storage effect is increased in the vertical **transistor** but reduced in the lateral **transistor**, the latter possessing increased collector efficiency.

L24 ANSWER 1 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 2002-074581 [10] WPIX
DNN N2002-055005 DNC C2002-022128
TI Fabrication of bipolar-complementary metal oxide semiconductor **integrated circuit** by out-diffusing impurities from surface conductors of **integrated circuit** into silicon **wafer**.
DC L03 U11 U13
IN ROBERTS, M C; VIOLETTE, M
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 2001031525 A1 20011018 (200210)* 10p
ADT US 2001031525 A1 Cont of US 1996-585453 19960116, US 2001-873808 20010604
FDT US 2001031525 A1 Cont of US 6245604
PRAI US 1996-585453 19960116; US 2001-873808 20010604
AB US2001031525 A UPAB: 20020213
NOVELTY - A bipolar-complementary metal oxide semiconductor (CMOS) **integrated circuit** is fabricated by out-diffusing impurities from surface conductors of the **integrated circuit** into the silicon **wafer** to form the **transistor** emitters.

DETAILED DESCRIPTION - Fabrication of bipolar-CMOS **integrated circuits** involves forming P-type and N-type **buried layers** in a silicon substrate, forming an **epitaxial layer** on top of the **buried layers**, forming P-type and N-type wells in the **epitaxial layer** over the different **conductivity type buried layers**, forming P-channel and N-channel MOS **transistors** in adjacent wells within the **epitaxial layer**, forming a first bipolar **transistor** within another well within the **epitaxial layer**, and connecting a layer of polysilicon at a first or second level of polysilicon to the bipolar **transistor** base to form by out-diffusion a bipolar **transistor** emitter region (124).

USE - For fabricating **integrated circuits** containing bipolar **transistors** and complementary metal-oxide-silicon **transistors**.

ADVANTAGE - The invention produces a maximum number of different **transistor** types using minimum number of individual integrated fabrication steps. It reduces manufacturing costs and enhances process yields, increases **integrated circuit** packing density, and improves bipolar **transistor** emitter connections.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional of a process step of the invention.

Emitter region 124

Dwg.2/4

L24 ANSWER 2 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1998-002069 [01] WPIX
DNN N1998-001613 DNC C1998-000782
TI Fabrication of **buried layers** in an integrated semiconductor device - with introduction of boron and phosphorus and arsenic/antimony impurities into a monocrystalline silicon substrate.
DC L03 U11 U13
IN GALBIATI, P; PALMIERI, M; VECCHI, L
PA (SGSA) SGS THOMSON MICROELTRN SRL
CYC 6

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PI   EP 809286      A1 19971126 (199801)* EN    8p
         R: DE FR GB IT
     JP 10055976    A  19980224 (199818)        6p
     US 5789288     A  19980804 (199838)
ADT  EP 809286 A1 EP 1996-830280 19960514; JP 10055976 A JP 1997-79041
     19970312; US 5789288 A US 1997-854584 19970512
PRAI EP 1996-830280    19960514
AB   EP     809286 A UPAB: 19990113
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A process for the fabrication of an integrated semiconductor device on a substrate of monocrystalline Si of first **conductivity type** (P), comprising the following steps: (a) introducing doping impurities of a first type (B) and a second type (P, As/Sb) through first and second areas respectively of the substrate (50); (b) subjecting the substrate to epitaxial growth at a high temperature to form on its main surface an **epitaxial layer** delimited by the buried regions of first **conductivity type** (p) and of second **conductivity type** (n) by diffusion of the impurities introduced; and (c) selectively doping the **epitaxial layer** so as to form a number of regions of p- and n-type. The process of introducing doping impurities of a first type (B) and a second type (P, As/Sb) into this consists of the following: (i) forming a mask (52) of SiN on the main surface of the substrate, leaving areas of the substrate exposed; (ii) introducing doping impurities of the second type (P) into the exposed areas of the substrate; (iii) forming a mask (54) of a material impervious to implantation of ions to leave a part of the substrate coated with SiN mask exposed; (iv) performing a first **ion-implantation** of doping impurities of a second type (As/Sb) with energy insufficient to traverse the SiN mask, but sufficient to introduce ions into the substrate through the remainder of the area of the substrate coated with SiN mask exposed; (v) performing a second **ion-implantation** with doping impurities of a second type (As/Sb) with energy sufficient to traverse the SiN mask to introduce ions into the substrate through the whole of the area of the substrate coated with SiN mask exposed; (vi) removing the mask (54); (vii) subjecting the substrate to a high-temperature treatment in an oxidising environment to form pads (55) of SiO2 on the areas of substrate not covered by the SiN mask; (viii) removing the SiN mask to expose areas of the substrate delimited by the pads; (ix) performing a third **ion-implantation** of doping impurities of a first type (B) with energy insufficient to traverse the SiO2 pads, but sufficient to introduce ions into the areas of the substrate delimited by the pads; and (x) removing the SiO2 pads.

USE - Useful in the processing of semiconductor **wafers**, especially in the fabrication of **buried layers**.

ADVANTAGE - A structure having three buried regions can be fabricated, e.g. a structure containing a DMOS **transistor**, a CMOS pair and a vertical pnp **transistor**. The DMOS **transistor** has an n-type buried well less doped at its edges so it is able to support higher voltages. The CMOS pair has a p-type well formed partly by a buried region P+B.ISO formed in the same operation as the deep insulation regions, and an n-type well with variable distribution of impurity concentrations particularly favourable to good insulation against the adjacent p+ regions, and to optimum immunity against ''latch-up''.
Dwg.7-10/10

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L24  ANSWER 3 OF 27  WPIX (C) 2002 THOMSON DERWENT
AN   1991-241641 [33]    WPIX
DNN  N1992-138887        DNC C1992-084303
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TI   N-well forming for CMOS **transistor** converts N-type **ion**

**implanted** layer - which is formed by N-type ion in P-channel MOS **transistor** element forming area, to N-well by heat treatment
- NoAbstract Dwg 1/4.

DC L03 U11 U13
IN YOSHIDA, H
PA (NIDE) NEC CORP
CYC 2
PI JP 03155661 A 19910703 (199133)*
US 5114868 A 19920519 (199223)B 17p
ADT JP 03155661 A JP 1990-202698 19900731; US 5114868 A US 1990-561191 19900801
PRAI JP 1989-201647 19890802

L24 ANSWER 4 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1989-237194 [33] WPIX
CR 1989-196005 [27]; 1989-196013 [27]; 1989-196014 [27]; 1989-224805 [31]; 1990-047953 [07]
DNN N1990-064576 DNC C1990-036736
TI Method of fabricating semiconductor **integrated circuit** - providing accurate control of current amplification factor.
DC L03 U11 U12 U13
IN HAYASAKA, K; HUZINUMA, K; IDOH, N; KUBODA, D; SEKIKAWA, S; TAKETA, K
PA (SAOL) SANYO ELECTRIC CO
CYC 3
PI JP 01171263 A 19890706 (198933)* 5p
US 4898837 A 19900206 (199012)
KR 9204174 B1 19920530 (199349)
ADT JP 01171263 A JP 1987-331176 19871225; US 4898837 A US 1988-271748 19881115; KR 9204174 B1 KR 1988-15291 19881119
PRAI JP 1987-292415 19871119; JP 1987-292416 19871119; JP 1987-292420 19871119; JP 1987-320227 19871217; JP 1987-331176 19871225; JP 1987-320337 19871217
AB JP 01171263 A UPAB: 19940126
A method of fabricating a semiconductor **integrated circuit** comprises the steps of; 1) preparing a semiconductor substrate of a first **conductivity type**, 2) forming **buried layers** of a second **conductivity type** in regions of the substrate, 3) forming an **epitaxial layer** of the second **conductivity type**, covering the substrate and **buried layers**, 4) forming isolation regions of the first **conductivity type**, dividing the **epitaxial layer** into islands, 5) selectively implanting ions to form a base region of the first **conductivity type** of a vertical, bipolar **transistor** in a surface layer of one island, and to form a resistor region in a surface layer of another island, this step including a first and a second **ion-implantation**, 6) determining the impurity concn. of the resistor region by selectively doping impurities into the resistor region and the base region of the vertical, bipolar **transistor**, during the first **ion-implantation**, 7) determining the impurity concn. in the base region by selectively doping impurities into the base region during the second **ion-implantation**, 8) causing the above a impurities to diffuse to a predetermined depth in the base region, and 9) selectively difusing impurities into a surface layer of the base region, to form an emitter region of the vertical bipolar **transistor**.

USE/ADVANTAGE - The method is used to form a se semiconductor **integrated circuit** which includes a bipolar **transistor** and a reistor, and provides accurate control of the

current amplification factor of the **transistor**. (First major
country equivalent to J01171263-A)
Dwg.2H/6

L24 ANSWER 5 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1988-016045 [03] WPIX
DNN N1988-011980 DNC C1988-006997
TI Simultaneous bipolar and CMOS fabrication - using minimal no. of masks giving good yield of high performance devices.
DC L03 U11 U13
IN MANOLIU, J; TUNTASOOD, P
PA (FAIR-N) FAIRCHILD SEMI COND; (FAIH) FAIRCHILD SEMICONDUCTOR CORP; (NASC) NAT SEMICONDUCTOR CORP
CYC 8
PI EP 253724 A 19880120 (198803)* EN 13p
R: DE FR GB IT NL
JP 63080560 A 19880411 (198820)
US 5023193 A 19910611 (199126) 12p
US 5407840 A 19950418 (199521) 14p
KR 9512742 B1 19951020 (199851)
ADT EP 253724 A EP 1987-401631 19870710; JP 63080560 A JP 1987-176068 19870716; US 5023193 A US 1988-253946 19881003; US 5407840 A Cont of US 1986-887006 19860716, Cont of US 1988-253946 19881003, Cont of US 1991-697360 19910508, US 1992-925807 19920804; KR 9512742 B1 KR 1987-7684 19870716
FDT US 5407840 A Cont of US 5023193
PRAI US 1986-887006 19860716
AB EP 253724 A UPAB: 19930923

A process for the simultaneous fabrication of bipolar and complementary field effect **transistors** uses as little as 6 masks prior to the contact mask. with the first mask two impurities of opposite type to the substrate (such as phosphorus and arsenic on O-type silicon) are implanted where **buried layers** are to be formed.An overall P-type cover and an undoped silicon **epitaxial layer** follow. Using the second mask this is N-doped (27,28) over the **buried layers**. the structure is then heated to 1050-1100 deg.C in nitrogen for 1-2 hrs. to diffuse the P and N impurities used to form the **buried layers** and wells. With the third mask the required field oxide regions are defined.

Following the front-end process, the minimum mask back-end process begins with a fourth mask to define the bipolar **transistor** base by boron **ion implantation**. The fifth mask defines the gate electrodes of polycrystalline Si deposited by chemical vapour disposition and doped with phosphorus to improve its conductivity. The NMOS source and drain regions and the bipolar device emitter and collector are defined by the sixth mask using arsenic **ion implantation**. The structure is then annealed at 900 deg.C, oxidised and electrical connections made. An alternative back-end process employs more masks but gives higher performance **transistors**.

USE/ADVANTAGE - The desirable integration of bipolar-and CMOS-forming processes on a single **wafer** is currently complex and lengthly, with many masking steps and may lead to poor yields. The new process uses a minimal number of masking steps yet results in high performance devices. It allows CMOS devices with a 1 micron gate while providing high-speed switching bipolar devices.
3/14

L24 ANSWER 6 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1985-115917 [19] WPIX

DNN N1985-087155 DNC C1985-050162
TI Diffused isolation regions in **ICS** - are formed by implanting fast diffusing impurity and diffusing through thin epilayer by heating.
DC L03 U11
IN KHADDER, W N; KRISHNA, S; RAMDE, A R
PA (NASC) NAT SEMICONDUCTOR INC
CYC 1
PI US 4512816 A 19850423 (198519)* 4p
ADT US 4512816 A US 1984-602264 19840423
PRAI US 1980-149203 19800512; US 1982-352630 19820226; US 1984-602264 19840423
AB US 4512816 A UPAB: 19930925
Insolation regions are formed in a monolithic **IC** including active **transistors** having emitter, base and collector regions by (a) depositing a thin first **conductivity type** epitaxial semiconductor layer (11) on an opposite type substrate (10) having a slow diffusing impurity contg. **buried layer** (12); (b) forming a masking oxide (13) over the **buried layer**; (c) removing the mask where isolation regions and **transistor** base regions are to be formed; (d) temporarily masking the base regions (31); (e) **ion implanting** a fast diffusing impurity into isolation areas; and (f) heating to diffuse the implanted impurity completely through the **epitaxial layer**.

ADVANTAGE - The isolation diffusion is conducted so penetration of the **buried layer** into the epilayer is minimised, allowing the epilayer thickness to be reduced to about 9 micron (40% redn). Lateral diffusion of the isolation impurity is also reduced, allowing a circuit density to be increased by as much as 40% or more.
3,4/7

L24 ANSWER 7 OF 27 WPIX (C) 2002 THOMSON DERWENT
AN 1983-724624 [31] WPIX
DNN N1983-133452 DNC C1983-072374
TI Forming semiconductor device for VLSI circuits - with vertical and lateral **transistors** formed during one step sequence.
DC L03 U11 U13
IN BERRY, R L; KO, W C
PA (FAIH) FAIRCHILD CAMERA CORP
CYC 8
PI EP 84500 A 19830727 (198331)* EN
R: DE FR GB IT NL
JP 58127368 A 19830729 (198336)
US 4433471 A 19840228 (198411)
CA 1205574 A 19860603 (198627)
EP 84500 B 19890524 (198921) EN
R: DE FR GB IT NL
DE 3379926 G 19890629 (198927)
ADT EP 84500 A EP 1983-400114 19830118; US 4433471 A US 1982-340395 19820118
PRAI US 1982-340395 19820118
AB EP 84500 A UPAB: 19930925
Method comprises (i) forming on a substrate of second **conductivity type** in succession (a) a buried interconnect layer of first (opposite) **conductivity type** over a selected region of the substrate; (b) **epitaxial layer** of first **conductivity type** partly overlying **buried layer**; (c) thin first oxide layer; (d) nitride layer; (e) grooves in portions of **epitaxial layer** form recessed islands of semiconductor material; (ii)

implanting a selected impurity into the exposed surfaces of grooves to form second **conductivity type** regions of higher impurity concn. than substrate, to prevent leakage currents in the structure to be formed; (iii) thermally oxidising the Si exposed in grooves forming second oxide layers directly contacting regions of the buried contact layer; (iv) removing selected portions of the nitride layer exposing parts of the first oxide layer covering portions of the island of semiconductor where further impurities are not added; (v) oxidising the **wafer** to form thick third oxide layer in regions exposed by removal of nitride; (vi) removing the rest of the nitride layer; (vii) masking to prevent impurity implantation in semiconductor material underlying mask which covers at least the contact region to the buried interconnect layer and the base of a lateral **transistor** to be formed; (viii) **ion implanting** second **conductivity type** impurity to form emitter and collector of **transistor**; (ix) removing the mask and forming a second mask to prevent implantation of impurities into the emitter and collector and the base contact of a vertical **transistor**; (x) **ion implanting** regions of first **conductivity type** not covered by the thin first oxide or second mask or thick oxide layers to form contact region to **buried layer** and emitters of vertical **transistor**; (xi) removing the second mask; and (xii) etching to **wafer** for long enough to remove the first oxide layer but not to damage second and third oxide layers thus opening selected contact areas to active regions of the devic

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L24  ANSWER 8 OF 27  WPIX (C) 2002 THOMSON DERWENT
AN   1982-66276E [32]   WPIX
TI   Transistor structure - formed inside IC housing.
DC   L03 U11 U12 U13
IN   TONNEL, E
PA   (CSFC) THOMSON CSF
CYC  6
PI   EP 57126      A  19820804 (198232)* FR   17p
         R: DE FR GB IT NL
     FR 2498812    A  19820730 (198238)
     JP 57143843   A  19820906 (198241)
     EP 57126      B  19880817 (198833)  FR
         R: DE FR GB IT NL
     DE 3278925    G  19880922 (198839)
ADT  EP 57126 A EP 1982-400081 19820118
PRAI FR 1981-1465       19810127
AB   EP      57126 A UPAB: 19930915
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**Transistor** structure, formed in a box of an **integrated circuit**, the base of which contains a localised **buried layer**, includes laterally isolated grooves filled with conductive material and cutting the pn junctions forming a wall of isolation (40) defining the box, while ensuring isolated contacts with the substrate (1) and isolated contacts (50,60) with the **buried layer** (23,33).

The dimensions of the isolating walls and the contact wells with the **buried layer** are reduced while the guard distance is cancelled and the effects on the **transistors** of parasitic fields are annulled.

2/8

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L24  ANSWER 9 OF 27  WPIX (C) 2002 THOMSON DERWENT
AN   1979-73471B [40]   WPIX
TI   Integrated circuit transistors prodn. -
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giving isolation and substrate connected collectors, using simultaneous out-diffusion to convert an **epitaxial layer**.

DC L03 U11 U12
IN COMPTON, J B
PA (NASC) NAT SEMICONDUCTOR INC
CYC 1
PI US 4168997 A 19790925 (197940)*
PRAI US 1978-949832 19781010
AB US 4168997 A UPAB: 19930901
Subsurface isolation layer is fabricated in an **integrated circuit** with the isolation layer spanned in selected regions by **buried layers**, by (a) **ion implanting** an impurity of first type into the selected regions of a substrate of first type impurity, (b) **ion implanting** a second impurity of opposite type into the substrate surface to a lower concn. than the first impurity, (c) growing an intrinsic **epitaxial layer**, and (d) processing the substrate to diffuse the second impurity through the **epitaxial layer** to determine is **conductivity type** and to diffuse the first impurity through the **epitaxial layer** to determine its **conductivity type** above the selected regions. The **epitaxial layer** is grown without deliberate impurity doping. Pref. the semiconductor is Si, the first impurity P and the second impurity B.
Method avoids the need for heavy doping and diffusion of the spanning **buried layers; transistors** produced may be isolated or substrate connected.

L24 ANSWER 10 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1995-326624 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE, AND SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN NANBA MITSUO
PA HITACHI LTD, JP (CO 000510)
PI JP 07326624 A 19951212 Heisei
AI JP1994-117804 (JP06117804 Heisei) 19940531
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 12
AB PURPOSE: To reduce a collector saturation resistance by introducing impurities of the same **conductivity type** in a plurality of times into a region for forming a collector **buried layer** of a bipolar **transistor** of a longitudinal structure formed on a semiconductor substrate.
CONSTITUTION: A semiconductor substrate 3 is constituted of a P-type single crystal and an **epitaxial layer** 4 constituted of an N-type Si single crystal is formed as an upper layer thereof. In a boundary region between the semiconductor substrate 3 and the **epitaxial layer** 4, a collector **buried layer** 5BL is formed. The collector **buried layer** 5BL is composed of a first collector **buried layer** 5BL1 and a second collector **buried layer** 5BL2 and antimony and arsenic being N-type impurities are introduced into the first collector **buried layer** 5BL1. The antimony being the N-type impurity is introduced into the second collector **buried layer** 5BL2. Since the impurity concentration of the collector **buried layer** can be made high thereby, a sheet resistance of the collector **buried layer** of a bipolar **transistor** of a longitudinal structure can be reduced without causing a defect or the like in the collector **buried**

**layer**.

L24 ANSWER 11 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1992-025067 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN SUGAI TOSHIYUKI
PA NEC YAMAGATA LTD, JP (CO 416643)
PI JP 04025067 A 19920128 Heisei
AI JP1990-126208 (JP02126208 Heisei) 19900516
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1198, Vol. 16, No. 188, P. 88 (19920507)
AB PURPOSE: To improve high frequency characteristic by incorporating steps of simultaneously forming a part in contact with a second **conductivity type** base region, an emitter region of a bipolar **transistor**, source and drain of a first MOSFET.
CONSTITUTION: Arsenic is **ion implanted** to a P-type semiconductor substrate 1 to form an N-type **buried layer** 2, boron is then **ion implanted** to form a P-type **buried layer** 3. Then, after an N-type **epitaxial layer** 4 is grown, boron is implanted to form P-type wells 5b in a P-type insulating layer 5a and a region 17 and a P-type first collector 5c in a region 16. Then, phosphorus is **ion implanted** to simultaneously form an N-type base 9a, a gate electrode 11 of polysilicon is formed on each MOSFET region, arsenic is **ion implanted** to simultaneously form source 8c, drain 8d of the region 17, a base contact 8b of the region 16 and emitter 8a of a region 15. Then, boron is implanted to simultaneously form source 10b, drain 10c of a region 18. The electrode 12 of each **transistor** is formed of Al to complete an **integrated circuit**. As a result, high frequency characteristics are improved.

L24 ANSWER 12 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1990-283029 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN KAWABATA KENICHI
PA FUJITSU LTD, JP (CO 000522)
PI JP 02283029 A 19901120 Heisei
AI JP1989-105052 (JP01105052 Heisei) 19890425
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1031, Vol. 15, No. 54, P. 81 (19910208)
AB PURPOSE: To form a main part of a **transistor** structure by using one mask by a method wherein, by side-etching a mask which has been used for field oxidation, a base leading-out electrode is formed, and then an emitter region is formed.
CONSTITUTION: On a semiconductor **wafer** 10 provided with a **buried layer** 2 of an inverse **conductivity type** and an **epitaxial layer** 3 of an inverse **conductivity type** on a semiconductor substrate 1 of a **conductivity type**, masks of a nitride film 4a and a oxide film 5a are formed, and a thick field oxide mask 8 is formed by performing field oxidation. After the field oxidation, by side- etching the masks of the nitride film 4a and the oxide film 5a, small masks 4b, 5b whose side surfaces are retreated are formed, and a part of the surface of the **epitaxial layer** 3 is exposed. By applying a bias voltage to the semiconductor **wafer**, silicon Si is subjected to bias sputtering. The whole surface of a polycrystalline silicon film 9 which is grown so as to have a flat surface is etched, and the masks of the nitride film 4b and the oxide film 5b are exposed.

L24 ANSWER 13 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1990-130868 JAPIO
TI SEMICONDUCTOR DEVICE
IN ITO TAKAHIRO; YAMAKI BUNSHIROU; YAMAMOTO YOSHIO
PA TOSHIBA CORP, JP (CO 000307)
PI JP 02130868 A 19900518 Heisei
AI JP1988-284772 (JP63284772 Heisei) 19881110
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 961, Vol. 14, No. 365, P. 89 (19900808)
AB PURPOSE: To reduce the source resistance of a MOS type field effect element and to improve high frequency gain by forming a high concentration impurity second **conductivity type buried layer** on a first **conductivity type** first **epitaxial layer** containing lower concentration impurity than that of a semiconductor substrate, and forming a first **conductivity type** second **epitaxial layer** containing lower concentration impurity than that of the substrate thereon.
CONSTITUTION: A first **conductivity type** first **epitaxial layer** 33 containing lower concentration impurity than that of a first **conductivity type** semiconductor substrate 32 containing high concentration impurity is formed on the substrate 32. A second **conductivity type buried layer** 11 containing high concentration impurity is formed on the layer 33. Further, a MOS type field effect element and a bipolar **transistor** are formed with a **wafer** having a structure in which a first conductivity second **epitaxial layer** 2 containing lower concentration impurity than that of the substrate 32 is formed on the layers 11 and 33. The source resistance of the element is reduced to enhance high frequency gain by employing the **wafer** of such a structure, thereby reducing its NF.

L24 ANSWER 14 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1990-094557 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN ITAGAKI ISAO
PA NEC YAMAGATA LTD, JP (CO 416643)
PI JP 02094557 A 19900405 Heisei
AI JP1988-246506 (JP63246506 Heisei) 19880930
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 944, Vol. 14, No. 292, P. 88 (19900625)
AB PURPOSE: To set Wepi directly under a second base region to about 0, and to improve the operating velocity of a large current by forming a first **conductivity type** second **buried layer** in contact with a second base region directly under the second base region on a first **buried layer**.
CONSTITUTION: Sb or As is diffused from the surface of a P- type substrate 1 of 1014-1016cm-3 to form an N+ type first **buried layer** 2, it is diffused or **ion implanted** from the surface of the layer 2 to form a P-type second **buried layer** 3. Further, an N- type **epitaxial layer** 4 is grown thereon, B is, for example, **ion implanted** from the surface of the layer 4 to simultaneously form P+ type injector region 8a, P+ type second base region 8b of an I2L having higher concentration and shallower than those of a first base region 6, and P+ type base region 8a of a normal NPN **transistor**. The region 8b is so formed as to be brought into contact with the layer 3. Since the same layer 3 as that of the region 8b is formed on the layer 2 directly under the region 8b to be brought into contact with the layer 3, a condition that Wepi directly

under the region 8b.simeq.0 can be realized. Accordingly, the storage of holes in the layer 4 directly under the region 8b can be ramarkably reduced to improve its operating velocity and particularly the operating velocity with a large current.

L24 ANSWER 15 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1989-283869 JAPIO
TI MANUFACTURE OF BIPOLAR **TRANSISTOR** FOR SEMICONDUCTOR **INTEGRATED CIRCUIT**
IN MEGURO KEN; TAKATSUKA ICHIRO
PA FUJI ELECTRIC CO LTD, JP (CO 000523)
PI JP 01283869 A 19891115 Heisei
AI JP1988-112881 (JP63112881 Heisei) 19880510
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 884, Vol. 14, No. 65, P. 34 (19900206)
AB PURPOSE: To reduce a diffusing step by simultaneously diffusing a base layer for forming a **transistor** together with an isolating layer for isolating a junction from a substrate at a region for forming the bipolar **transistor**.
CONSTITUTION: A first diffusing step of diffusing other **conductivity type** impurity for a **buried layer** 2 of one **conductivity type** semiconductor substrate 1, and an epitaxially growing step of growing an **epitaxial layer** 4 in the other **conductivity type** as a collector region 9 thereon are provided. Further, a second diffusing step of simultaneously diffusing an isolating layer 5 for junction- isolating the region 9 from the substrate 1 from the surface of the layer 4 around the layer 2 and a base layer 6 disposed at the upper side of the layer 2 in one **conductivity type**, and a third diffusing step of diffusing an emitter layer 7 from the surface of the layer 6 in the other **conductivity type** are provided. Thus, a bipolar **transistor** is associated. Thus, the number of diffusing steps which was heretofore required for four times at the minimum may be three times, thereby reducing its cost.

L24 ANSWER 16 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1989-161764 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR **INTEGRATED CIRCUIT**
IN HAYASAKA KATSUHIRO; SEKIKAWA NOBUYUKI; KUBOTA TETSUYA; FUJINUMA CHIKAO
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
PI JP 01161764 A 19890626 Heisei
AI JP1987-320227 (JP62320227 Heisei) 19871217
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 824, Vol. 13, No. 433, P. 118 (19890927)
AB PURPOSE: To control hFE of an N-P-N **transistor** in a semiconductor in tegrated circuit, into which a resistance element through **ion implantation** is incorporated, by conducting **ion implantation** forming a resistance region prior to emitter diffusion and the introduction of an impurity into a base region, shaping a CVD oxide film onto the surface and driving in the base region.
CONSTITUTION: Reverse **conductivity type buried layers** 22 are formed to one **conductivity type** semiconductor substrate 21, and a reverse **conductivity type epitaxial layer** 23 is shaped onto the substrate 21 and isolated into a plurality of islands 25. The ions of one **conductivity type** impurity forming a resistance region 28 prior to emitter diffusion are implanted to one island surface, and one **conductivity type** impurity shaping a base region 29 is introduced into another island region. The surface of the base region 29

exposed is coated with a CVD oxide film 33, the whole substrate is thermally treated, and the base region 29 is diffused up to specified depth. A reverse **conductivity type** impurity is diffused selectively from the surface of said **epitaxial layer** 23 and an emitter region 34 is shaped, and hFE of a vertical type bipolar **transistor** is controlled at a fixed value through heat treatment.

L24 ANSWER 17 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1989-161749 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR **INTEGRATED CIRCUIT**
IN SEKIKAWA NOBUYUKI; TAKADA TADAYOSHI; NISHIDA OSANORI; FUJINUMA CHIKAO
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
PI JP 01161749 A 19890626 Heisei
AI JP1987-320229 (JP62320229 Heisei) 19871217
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 824, Vol. 13, No. 433, P. 113 (19890927)
AB PURPOSE: To solve the difficulty of the control of hFE of an N-P-N **transistor** by incorporating a MIS type capacitance and a resistance element through **ion implantation** by forming a lower electrode region in the MIS type capacitance and a resistance region through **ion implantation** prior to emitter diffusion.
CONSTITUTION: Reverse **conductivity type buried layers** 22 are shaped to one **conductivity type** semiconductor substrate 21, reverse **conductivity type epitaxial layers** 24 are formed onto the layers 22, and the whole is isolated into a plurality of islands 25. A lower electrode region 28 in a MIS type capacitance is shaped to the surface of one island 25, and one **conductivity type** resistance region 30 and a base region 31 in one **conductivity type** vertical type bipolar **transistor** are formed respectively to the surfaces of other islands 25. A partial region in the surface of the lower electrode region 28 is exposed, a dielectric thin-film 35 in the MIS type capacitance is shaped onto the surface of the region, and a reverse **conductivity type** impurity is diffused selectively and an emitter region 36 is diffused up to specified depth. A conductor film is formed onto the whole surface, and an upper electrode 39 in the MIS type capacitance is disposed onto the dielectric thin film 35 and electrodes 38 to the desired sections of the surfaces of each region respectively.

L24 ANSWER 18 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1988-239861 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN KOBAYASHI YUTAKA; IKEDA TAKAHIDE; HORI RYOICHI; KITSUKAWA GORO; ITO KIYOO; TANBA NOBUO; WATABE TAKAO
PA HITACHI LTD, JP (CO 000510)
PI JP 63239861 A 19881005 Showa
AI JP1987-71414 (JP62071414 Showa) 19870327
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 710, Vol. 13, No. 44, P. 133 (19890131)
AB PURPOSE: To highly integrate a semiconductor **integrated circuit** device against a software error and adapted for high speed operation with low power consump tion by forming a reverse **conductivity type** semiconductor region under the semiconductor region of a circuit element of the semiconductor region or periph eral circuit for forming a memory cell circuit element.
CONSTITUTION: A DRAM memory cell is composed of a series circuit of a

switch n-channel MOSFETQs and a capacity element Cp. A **buried layer** 3 of the same **conductivity type** as that of a semiconductor substrate 1 and higher impurity concentration is formed between the substrate 1 and an **epitaxial layer** 2 under the memory cell. Thus, a potential barrier is formed for minority carrier generated in the substrate 1 under the MISFETQs or the element Cp by minority carrier and alpha-ray implanted from an n+ type semiconductor region disposed in the vicinity to the substrate by the operation of a parasitic bipolar **transistor**. Accordingly, it can prevent the minority carrier from invading to the memory cell. Thus, an access time can be accelerated, and it can prevent a software error, and improves its electric reliability.

L24 ANSWER 19 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1988-047965 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT**
IN OKODA TOSHIYUKI
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
PI JP 63047965 A 19880229 Showa
AI JP1986-193467 (JP61193467 Showa) 19860818
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 637, Vol. 12, No. 265, P. 10 (19880723)
AB PURPOSE: To easily allow a high speed IIL, a vertical P-N-P **transistor** having preferable characteristics and an N-P-N **transistor** to integrally coexist by composing the emitter of the vertical **transistor** of a shallower emitter region than the base region of the N-P-N **transistor**.
CONSTITUTION: On one **conductivity type** semiconductor substrate 21 are formed a reverse **conductivity type** **epitaxial layer** 22, reverse **conductivity type** first **buried layers** 23a, 23b, a second **buried layer** 23c formed deeply to the substrate 21 in lower impurity concentration than the layers 23a, 23b, and one **conductivity type** separating region 24. An IIL in which its base is composed of a buried base region 26 is formed, and a normal **transistor** is formed on a second insular region 25b. On a third insular region 25c are formed one **conductivity type** collector **buried layer** 34 buried by overlapping it on the layer 23c, a reverse **conductivity type** base region 35, one **conductivity type** collector leading region 36, a reverse **conductivity type** base contact region 37 and one **conductivity type** emitter region 38 shallower than the region 31 formed on the surface 25b, thereby forming a vertical **transistor**.

L24 ANSWER 20 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1987-156866 JAPIO
TI SEMICONDUCTOR DEVICE
IN HARA TOMOOKI
PA NEC CORP, JP (CO 000423)
PI JP 62156866 A 19870711 Showa
AI JP1985-293541 (JP60293541 Showa) 19851228
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 568, Vol. 11, No. 396, P. 43 (19871224)
AB PURPOSE: To extend a depletion layer in a P-N junction easily and improve a dielectric strength and facilitate application to a power semiconductor **integrated circuit** by a method wherein one **conductivity type** 3rd **buried layer** with an intermediate concentration between 1st **buried**

**layer** and 2nd **buried layer** is provided in a boundary region between the 1st **buried layer** and the 2nd **buried layer**.
CONSTITUTION: 31P+ ions and 11B+ ions are implanted into the surface of a P- type semiconductor substrate 1 to form N-type 1st **buried layer** 2 and P-type 3rd **buried layer** 3 respectively. Then BCl3 is diffused to form P+ type 2nd **buried layers** 4 and an N- type **epitaxial layer** 5 is made to grow and P-type 2nd collector region 6, P+ type 3rd collector region 7a and P+ type insulating isolation region 7b are formed simultaneously. Then an N+ type base region 8, a P+ type emitter region 9a, a P+ type collector contact region 9b, an N+ type base contact region 10a and an N+ type bias contact region 10b are formed to complete a triple diffusion type PNP **transistor** QPNP1.

L24 ANSWER 21 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1986-292355 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT**
IN TAKATSUKA ICHIRO; NAGAYASU YOSHIHIKO; SHIGETA YOSHIHIRO
PA FUJI ELECTRIC CO LTD, JP (CO 000523)
PI JP 61292355 A 19861223 Showa
AI JP1985-133723 (JP60133723 Showa) 19850619
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 508, Vol. 11, No. 154, P. 107 (19870519)
AB PURPOSE: To hardly cause a latchup by forming a **conductive type** MOS **transistor** of the same semiconductor between a source and a drain as an epitaxially grown layer in the same **conductive type** higher density impurity diffused region as the grown layer to enhance the withstand voltage of a bipolar **transistor** without varying CMOS characteristics.
CONSTITUTION: An N-type **epitaxial layer** 2 is formed on a P-type silicon substrate 1, and an N-type **buried layer** 6 is formed on a partial region. When boron ions 21 and phosphorus ions 22 are implanted to drive-in to be diffused, a collector wall 5, an isolation 7, a P-well 10 and an N-well 13 are formed. A gate oxide film 15, N-type source/drain 8, 9 of an N-channel MOS **transistor**, P-type source/drain 11, 12 of P-channel MOS **transistor**, a gate electrode 14 and base, 3, emitter 4 of N-P-N **transistor** are formed completely The P-channel MOS **transistor** is formed in the N-well of high impurity density and low specific resistance by the epitaxially grown layer.

L24 ANSWER 22 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1986-206251 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN KAWAKATSU AKIRA
PA OKI ELECTRIC IND CO LTD, JP (CO 000029)
PI JP 61206251 A 19860912 Showa
AI JP1985-46399 (JP60046399 Showa) 19850311
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 478, Vol. 11, No. 41, P. 13 (19870206)
AB PURPOSE: To obtain high gains with excellent reproducibility while enabling operation at high speed, and to improve load driving capability by forming a first **conduction type** third region diffused from the surface of an **epitaxial layer** to the side surface of a second region and demarcating the side surface and base of an **epitaxial layer** in an island region by the second region and the third region.
CONSTITUTION: An N+ type buried diffusion layer 2 is shaped to a P- type

silicon substrate 1, an silicon oxide film 10 is formed, and boron ions are implanted while using a resist 11 as a mask, and annealed in an inactive atmosphere. An N-type **epitaxial layer** 4 is shaped, and isolated by an element isolation silicon oxide film 3. Boron is buried into the N+ type **buried layer** 2 in high concentration as a rule at that time, and an active P-type layer is not formed yet. An inactive P-type layer 51 is diffused and shaped to the N-type **epitaxial layer** 4, boron made to be contained in the buried diffusion layer 2 is diffused upward through the heat treatment of the layer 4 to form an active P-type layer 52, and an N-type layer 6 is isolated from the **epitaxial layer** 4. A P+ type layer 7 is diffused and shaped, and the opening of an N+ layer for the ohmic contact of the N-type layer 6 is bored. The current gains of a PNP **transistor** are controlled by the diffusion depth of the P+ type layer 7.

L24 ANSWER 23 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1985-250664 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE AND MANUFACTURE THEREOF
IN IWASAKI HIROSHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 60250664 A 19851211 Showa
AI JP1984-106777 (JP59106777 Showa) 19840526
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 400, Vol. 1, No. 117, P. 38 (19860502)
AB PURPOSE: To prevent a latchup phenomenon in a CMOS part from occurring by burying a high impurity density layer under a well formed with the first **conductive type** IGFET and providing a protecting ring of the second **conductive type** high impurity density arriving at the **buried layer**.
CONSTITUTION: A p type **epitaxial layer** on a p type Si substrate 11 is divided by an N+ type **buried layer** 12 and an N type well 14, and separated by channel cuts 18, 19 and a thick oxide film. Ions are implanted through a gate oxide film, and a p type layer 23 is formed and a threshold value adjustments 24, 25 are performed. A window 29 is opened, no-addiion polysilicon 28 is coated, a window 291 is masked with SiO2 30, P is diffused to provide N+ type layers 26, 27 arriving at the layer 12, the mask 30 is then removed, and As is diffused. Electrodes 31-34 provided from the layer 28, and an N+ type layer is formed from the electrode 33. Then, As, B are selectively implanted to form CMOS FET and the P+ type base leading layer 40 of a bipolar element, and the layer 26 is maintained at the highest potential. With this configuration, the current amplification factors .beta.1, .beta.2 of the parasitic bipolar **transistors** of the CMOS are small, and set to .beta.1, .beta.2<1, thereby preventing latchup.

L24 ANSWER 24 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1985-229361 JAPIO
TI SEMICONDUCTOR INJECTION INTEGRATED **LOGIC CIRCUIT** DEVICE
IN OOKODA TOSHIYUKI
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
TOKYO SANYO ELECTRIC CO LTD, JP (CO 323368)
PI JP 60229361 A 19851114 Showa
AI JP1984-85381 (JP59085381 Showa) 19840426
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 392, Vol. 1, No. 82, P. 141 (19860402)
AB PURPOSE: To prevent the lowering of the reverse current factor of a

reverse vertical type **transistor** by forming a well region having impurity concentration higher than a **buried layer** to the surface of the **buried layer** and shaping a collector region to the surface of the well region through a base region.
CONSTITUTION: A reverse **conduction type** well region 25 having impurity concentration higher than an **epitaxial layer** 24 on reverse **conduction type buried layers** 22, 23 is formed to the surface of the **epitaxial layer** 24, and reverse **conduction type** collector regions 26 are shaped to the surface of the region 25 through a base region 29, thus constituting a reverse vertical type **transistor**. Since a gate grounding type J-FETT1 is connected to the reverse vertical type **transistor** TR while being used as an injector, the VBE voltage of the **transistor** TR applies a bias to a gate in the FETT1, thus improving the constant-current operation of the FETT1.

L24 ANSWER 25 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1985-180165 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN TASHIRO TSUTOMU
PA NEC CORP, JP (CO 000423)
PI JP 60180165 A 19850913 Showa
AI JP1984-35533 (JP59035533 Showa) 19840227
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 376, Vol. 1, No. 2, P. 47 (19860125)
AB PURPOSE: To obtain the titled device including a bipolar **transistor** having high performance with a diffusion layer, a junction thereof is shallow and small, by forming an emitter region consisting of a first **conduction type epitaxial layer**, a side surface thereof is coated with an insulating film, and a second **conduction type** base region interposing between the nose of the emitter region and a first insular region.
CONSTITUTION: A **buried layer** 2 and a growth layer 3 are formed on a silicon substrate 1, a foundation oxide film 4 and a nitride film 5 are shaped on the layer 3, and an insulating isolation oxide film 6 is formed through selective oxidation. A diffusion layer 7 and a base diffusion layer 8 are shaped, a doped polycrystalline silicon film 9 is grown, and formed so as to selectively cover the diffusion layer 8, and a CVD oxide film 10 is shaped. A selective **epitaxial layer** 13 to which arsenic is doped is formed, and boron is diffused from the polycrystalline silicon film 9 to shape a contact base diffusion layer 12 having low resistance. A protective film 14 is formed, and an Al electrode 15 is shaped. Heat treatment at a high temperature is required only when the selective epitaxial growth layer as an emitter is shaped, and a junction, the depth of a base junction thereof is extremely shallow, can be formed.

L24 ANSWER 26 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1985-124860 JAPIO
TI SEMICONDUCTOR DEVICE
IN OSHIMA JIRO; KO TATSUICHI; ABE MASAYASU; YASUJIMA TAKASHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 60124860 A 19850703 Showa
AI JP1983-231263 (JP58231263 Showa) 19831209
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 356, Vol. 9, No. 28, P. 154 (19851108)
AB PURPOSE: To reduce the variation of the position of the interface due to

an autodoping phenomenon, and to obtain the stable effective layer thickness of an **epitaxial layer** by forming an impurity region having a **conduction type** reverse to the **epitaxial layer** to the surface layer section of an silicon substrate as a **buried layer**.
CONSTITUTION: A P+ **buried layer** 9 having a **conduction type** reverse to an **epitaxial layer** 2 is formed to a substrate surface-layer section between a collector **buried layer** 7 in a first **transistor** and a collector **buried layer** 8 in a second **transistor** in a CFL circuit incorporated into a bipolar **IC** . The **buried layer** 9 differs from **buried layers** 3, 7, 8 separately formed to an **IC** and is not connected to the surface of the **epitaxial layer** 2.
Impurity concentration in the impurity region 9 is made sufficiently higher than that scattering by an autodoping phenomenon, the position of the interface is controlled by impurity atoms in the impurity region, and variance due to autodoping atoms is inhibited.

L24 ANSWER 27 OF 27 JAPIO COPYRIGHT 2002 JPO
AN 1980-133552 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT**
IN KISHI TADASHI
PA NEC CORP, JP (CO 000423)
PI JP 55133552 A 19801017 Showa
AI JP1979-40126 (JP54040126 Showa) 19790403
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 40, Vol. 5, No. 31, P. 54 (19810110)
AB PURPOSE: To provide a universal **integrated circuit** simply in high integrity by forming an island region of the same **conducting type** as a high impurity density **buried layer** directly over a high impurity density buried region in a semiconductor substrate, making the island region contact with the **buried layer** and thus forming a **transistor**, resistors and the like on the island region.
CONSTITUTION: An n+type **buried layer** 2 is selectively formed on the surface of a p-type semiconductor substrate 1. A p-type **epitaxial layer** 3 is then formed thereon, and an n-type region 4 is formed by an **ion implantation** process.
Unit functions of npn **transistor**, diode, resistors and the like are then formed in the n-type **ion implanted** region 4.
A resistor 9 and a MOS **transistor** 10 as also formed on the region where n-type ion is not implanted of the layer 3. An isolation is conducted by thick oxide films 5. Thus, the **epitaxial layer** of the same **conducting type** as the substrate is formed to form an island region therein by a simple electric isolation to reduce the margin in designing it so as to enhance the integrity of the semiconductor **integrated circuit**.

L41 ANSWER 1 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1995-242169 [32] WPIX
DNN N1995-188782
TI High voltage, high beta bipolar **transistor** for
**integrated circuit** esp. NPN **transistor** in
n-well BiCMOS - Has collector region extending through lightly doped
region to collector buried layer disposed below lightly doped region..
DC U12
IN CORSI, M; HUTTER, L N
PA (TEXI) TEXAS INSTR INC
CYC 6
PI EP 662717 A2 19950712 (199532)* EN 35p <--
R: DE FR GB IT NL
EP 662717 A3 19950802 (199613) <--
US 5614755 A 19970325 (199718) 23p <--
ADT EP 662717 A2 EP 1994-106859 19940502; EP 662717 A3 EP 1994-106859
19940502; US 5614755 A US 1993-56446 19930430
PRAI US 1993-56446 19930430
AB EP 662717 A UPAB: 19950818
The bipolar **transistor** includes a base region (55) of a lightly doped p-type semiconductor layer (44). A collector includes a collector region (50) and a buried layer (48). The lightly doped layer is formed over the buried layer.

The collector region is n-type semiconductor material and extends through the lightly doped layer to contact the buried layer. Pref. the collector region isolates the lightly doped base region (52). The base region pref. includes two different doping level regions. An n-type emitter (66) is formed in the base region.

USE/ADVANTAGE - Structure suitable for Schottky diode. **Transistor** current gain maximised without use of extremely narrow base widths; avoids increased epilayer thickness to increase high voltage capability.
Dwg.5/36

L41 ANSWER 2 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1995-103396 [14] WPIX
DNN N1995-081507
TI Semiconductor **IC** apparatus with input protection circuit -
allows current to flow between input terminals by forming impurity domain
in one well and drain domain in another.
DC U13
IN MIZUKAMI, S
PA (TOKE) TOSHIBA KK; (TOSZ) TOSHIBA MICROELECTRONICS KK
CYC 3
PI JP 07029987 A 19950131 (199514)* 5p <--
US 5581103 A 19961203 (199703) 9p <--
KR 139873 B1 19980817 (200021) <--
JP 3246807 B2 20020115 (200206) 7p <--
ADT JP 07029987 A JP 1993-168053 19930707; US 5581103 A US 1994-271146
19940706; KR 139873 B1 KR 1994-16270 19940707; JP 3246807 B2 JP
1993-168053 19930707
FDT JP 3246807 B2 Previous Publ. JP 07029987
PRAI JP 1993-168053 19930707
AB JP 07029987 A UPAB: 19950412
The apparatus consists of an N+ type implanting layer (12) formed on the surface of a P type semiconductor substrate (11). P type wells (16,18) are formed in an epitaxial layer of the implanting layer. Both wells are

isolated by an N type well (17).
A MOST in the first well has one end grounded, another end and a gate (24) connected to an input terminal (36). A P+ type impurity domain (26) in the second well is grounded. When voltage is applied to the input terminal, a surge voltage is generated in the drain domain (25) and impurity domain (27), in the second well.
ADVANTAGE - Good input protection characteristic.
Dwg.1/5

L41 ANSWER 3 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1994-224589 [27] WPIX
CR 1993-008591 [01]
DNN N1994-177014 DNC C1994-103146
TI Vertical DMOS **transistor** built in an N-well MOS-based BICMOS - with both devices merged together on a **chip**, so avoiding tapered field oxide.
DC L03 U12 U13
IN ERDELJAC, J P; HUTTER, L N
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 5317180 A 19940531 (199427)* 18p <--
ADT US 5317180 A Div ex US 1990-592108 19901003, Cont of US 1991-755406 19910905, US 1992-876689 19920428
FDT US 5317180 A Div ex US 5171699
PRAI US 1990-592108 19901003; US 1991-755406 19910905; US 1992-876689 19920428
AB US 5317180 A UPAB: 19940824
An **IC** having plural active components including a DMOS **transistor** and a bipolar **transistor** comprises (a) a first P-type layer; (b) plural spaced apart N+ regions at a common surface of the first P-type layer, each N+ region corresponding with one of the plural active components; (c) plural spaced apart N-**well regions**, each being contiguous to one of the N+ regions, each of the N-**well regions** containing the current path of one of the active components; (d) wherein the N-well has a surface and wherein the DMOS **transistor** includes an N-type source and drain and a P-type backgate region in the N-well having a backgate opening with an edge at the surface of the N-well and a gate insulatingly spaced from the N-well defining the edge of the backgate opening at the surface of the N-well, the gate having a sidewall oxide defining an edge of an opening for the source at the surface of the N-well.
USE/ADVANTAGE - Used to integrate an n-channel vertical double diffused MOS (VDMOS) structure into an N-well CMOS-based bipolar CMOS process. Fabrication takes place from a CMOS point of view rather than from the bipolar point of view; the peripheral portion of the DMOS device is terminated by a PN junction, thereby avoiding the necessity of having a tapered field oxide.
Dwg.12/14

L41 ANSWER 4 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1993-001617 [01] WPIX
DNN N1993-001086
TI Semiconductor surface EEPROM cell with tunnel diode and sense **transistor** channel regions - has conductive control gate insulatively disposed over floating gate and thin tunnel insulator formed on semiconductor layer over tunnel diode region.
DC U13 U14 X22
IN SMAYLING, M C
PA (TEXI) TEXAS INSTR INC

CYC 9
PI EP 520825 A1 19921230 (199301)* EN 71p <--
R: DE FR GB IT NL
US 5225700 A 19930706 (199328) 67p <--
TW 201362 A 19930301 (199330) <--
JP 05235372 A 19930910 (199341) <--
EP 520825 B1 19961218 (199704) EN 71p <--
R: DE FR GB IT NL
DE 69215978 E 19970130 (199710) <--
KR 269078 B1 20001016 (200138) <--
JP 3265311 B2 20020311 (200220) 53p <--
ADT EP 520825 A1 EP 1992-305931 19920626; US 5225700 A US 1991-722812 19910628; TW 201362 A TW 1992-106220 19920806; JP 05235372 A JP 1992-171329 19920629; EP 520825 B1 EP 1992-305931 19920626; DE 69215978 E DE 1992-615978 19920626, EP 1992-305931 19920626; KR 269078 B1 KR 1992-11347 19920627; JP 3265311 B2 JP 1992-171329 19920629
FDT DE 69215978 E Based on EP 520825; JP 3265311 B2 Previous Publ. JP 05235372
PRAI US 1991-722812 19910628
AB EP 520825 A UPAB: 19930924
The non-stack EEPROM cell formed on a P-type semiconductor surface includes an N-type tunnel region spaced from two highly doped N-type regions (688, 701) terminating a sense **transistor** channel region (696). One insulator region (732) is formed over the tunnel diode region and another over the channel region.

A floating gate conductive layer (708) extends over the two insulator regions. A control gate (706) is superimposed over, but is insulated from, the floating gate, and overlaps the lateral margins of the latter at all points.

USE/ADVANTAGE - For e.g. automotive electrical systems. Provides highly reliable bit-programmable memory cell. Creates both high and low voltage semiconductor devices on single **chip**. (20,20g/25
20,20g/25

L41 ANSWER 5 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1991-174598 [24] WPIX
CR 1991-062915 [09]
DNN N1993-116945 DNC C1993-068210
TI Semiconductor device with insulated gates - having fast switching speed and excellent breakdown strength.
DC L03 U12
IN MORI, M; NAKANO, Y; YASUDA, Y
PA (HITA) HITACHI LTD
CYC 3
PI JP 03105980 A 19910502 (199124)* <--
US 5208471 A 19930504 (199319)B 15p <--
US 5262339 A 19931116 (199347) 14p <--
KR 173778 B1 19990201 (200038) <--
ADT JP 03105980 A JP 1989-242224 19890920; US 5208471 A Cont of US 1990-536521 19900612, US 1991-762793 19910919; US 5262339 A Cont of US 1990-536521 19900612, Div ex US 1991-762793 19910919, US 1993-17420 19930210; KR 173778 B1 KR 1990-8598 19900612
FDT US 5208471 A JP 03012970; US 5262339 A Div ex US 5208471
PRAI JP 1989-242224 19890920; JP 1989-146814 19890612
AB JP 03105980 A UPAB: 20000801
A semiconductor device comprises a) a semiconductor substrate (11) of first or second **conductivity type** and having a first main electrode (2) on one surface (101); b) a first semiconductor region (12) of first **conductivity type** (e.g. n-type) forming the upper main surface (102) of the substrate; c) several second

semiconductor regions (13) of p-type exposed at the upper surface and comprising parallel elongated regions; d) several insulated gate electrodes (4), each formed with an insulating film (5) interposed on upper surface (102) across portions of adjacent second semiconductor regions; e) third semiconductor regions (14) of n-type formed on the upper surface and extending into second semiconductor regions, so that part of each third semiconductor region is beneath an end of one of the insulated gate electrodes; f) a fourth semiconductor region (15) of p-type adjacent to and parallel to the end second semiconductor regions only and formed to extend deeper into region (12) and with a higher impurity concn. than the second semiconductor regions; g) a second main electrode (3) in contact with second and third semiconductor regions with a low resistance; and h) a means to connect electrically the second main electrode with the fourth semiconductor region. The contact between the second main electrode (3) and the end second semiconductor region is located at a peripheral side w.r.t. the contact between the said electrode and the end third semiconductor region.

USE/ADVANTAGE - Useful for mfg. semiconductor devices with insulated gates, esp. power MOSFET's and IGBTs. The invented devices can perform high speed switching, esp. fast turn-off, and have high insulation properties (i.e. excellent breakdown strength). The device prevents latch up due to parasitic thyristor or **transistor**. (First major country equivalent to JP3105980

L41 ANSWER 6 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1991-062915 [09] WPIX
CR 1991-174598 [24]
DNN N1991-048506
TI Semiconductor device with insulated gates - having fast switching speed and excellent breakdown strength.
DC L03 U12
IN MORI, M; NAKANO, Y; YASUDA, Y
PA (HITA) HITACHI LTD
CYC 3
PI JP 03012970 A 19910121 (199109)*
US 5208471 A 19930504 (199319)B 15p <--
US 5262339 A 19931116 (199347) 14p <--
KR 173778 B1 19990201 (200038) <--
ADT JP 03012970 A JP 1989-146814 19890612; US 5208471 A Cont of US 1990-536521 19900612, US 1991-762793 19910919; US 5262339 A Cont of US 1990-536521 19900612, Div ex US 1991-762793 19910919, US 1993-17420 19930210; KR 173778 B1 KR 1990-8598 19900612
FDT US 5208471 A JP 03012970; US 5262339 A Div ex US 5208471
PRAI JP 1989-146814 19890612; JP 1989-242224 19890920
AB JP 03012970 A UPAB: 20000725
A semiconductor device comprises a) a semiconductor substrate (11) of first or second **conductivity type** and having a first main electrode (2) on one surface (101); b) a first semiconductor region (12) of first **conductivity type** (e.g. n-type) forming the upper main surface (102) of the substrate; c) several second semiconductor regions (13) of p-type exposed at the upper surface and comprising parallel elongated regions; d) several insulated gate electrodes (4), each formed with an insulating film (5) interposed on upper surface (102) across portions of adjacent second semiconductor regions; e) third semiconductor regions (14) of n-type formed on the upper surface and extending into second semiconductor regions, so that part of each third semiconductor region is beneath an end of one of the insulated gate electrodes; f) a fourth semiconductor region (15) of p-type adjacent to and parallel to the end second semiconductor regions only and formed to

extend deeper into region (12) and with a higher impurity concn. than the second semiconductor regions; g) a second main electrode (3) in contact with second and third semiconductor regions with a low resistance; and h) a means to connect electrically the second main electrode with the fourth semiconductor region. The contact between the second main electrode (3) and the end second semiconductor region is located at a peripheral side w.r.t. the contact between the said electrode and the end third semiconductor region.

USE/ADVANTAGE - Useful for mfg. semiconductor devices with insulated gates, esp. power MOSFET's and IGBTs. The invented devices can perform high speed switching, esp. fast turn-off, and have high insulation properties (i.e. excellent breakdown strength). The device prevents latch up due to parasitic thyristor or **transistor**. (First major country equivalent to JP3105980

L41 ANSWER 7 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1991-052572 [08] WPIX
DNN N1991-040753
TI Semiconductor structure for high power **integrated circuits** - has two epitaxial layers each having patterned buried layer and third layer in which power, logic and analogic device are formed.
DC U11 U13
IN CAMBOU, B
PA (MOTI) MOTOROLA INC
CYC 6

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PI   EP 413256     A  19910220 (199108)*            <--
         R: DE FR GB IT
     JP 03088362   A  19910412 (199121)             <--
     US 5070382    A  19911203 (199151)             <--
     EP 413256     A3 19920722 (199335)             <--
     EP 413256     B1 20001011 (200052)  EN         <--
         R: DE FR GB IT
     DE 69033647   E  20001116 (200065)             <--
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ADT EP 413256 A EP 1990-115280 19900809; JP 03088362 A JP 1990-215941 19900817; US 5070382 A US 1989-395695 19890818; EP 413256 A3 EP 1990-115280 19900809; EP 413256 B1 EP 1990-115280 19900809; DE 69033647 E DE 1990-633647 19900809, EP 1990-115280 19900809
FDT DE 69033647 E Based on EP 413256
PRAI US 1989-395695 19890818
AB EP 413256 A UPAB: 19931119
The semiconductor structure comprises a substrate (20) of a first **conductivity type**; and an epitaixal layer (21) of a second **conductivity type**, disposed on the substrate (20) and having a buried layer (25) of a first **conductivity type**. A second epitaxial layer (26) of a second **conductivity type** is disposed on the first epitaxial layer (21) and has a second buried layer (30) of a first **conductivity type** which is formed over the first buried layer (25).

A third epitaxial layer (32) of a first **conductivity type** is disposed on the second epitaxial layer (26), and has isolation regions (33) extending down to the second epitaxial layer (26), and surrounding the first two buried layers (25, 26).

ADVANTAGE - Total thickness of first two epitaxial layers (21, 26) reduces NPN parasitic **transistor** effect. @(6pp Dwg.NO 3/4)@
3/4

L41 ANSWER 8 OF 30 WPIX (C) 2002 THOMSON DERWENT

AN 1990-356111 [48] WPIX
DNN N1990-272002
TI Monolithic semiconductor combining CCD, bipolar and MOS structures - has **transistor** formed in top of three layers formed in substrate with preset doping profile.
DC U13
IN KIHARA, K; TAGUCHI, M
PA (TOKE) TOSHIBA KK
CYC 6
PI EP 399454 A 19901128 (199048)* 18p <--
R: DE FR GB
US 4994888 A 19910219 (199110) 16p <--
JP 03114235 A 19910515 (199126) <--
KR 9302296 B1 19930329 (199419) <--
EP 399454 B1 19980422 (199820) EN 22p <--
R: DE FR GB
DE 69032255 E 19980528 (199827) <--
ADT EP 399454 A EP 1990-109682 19900522; US 4994888 A US 1990-525040 19900518; JP 03114235 A JP 1989-128314 19890522; KR 9302296 B1 KR 1990-7350 19900522; EP 399454 B1 EP 1990-109682 19900522; DE 69032255 E DE 1990-632255 19900522, EP 1990-109682 19900522
FDT DE 69032255 E Based on EP 399454
PRAI JP 1989-128314 19890522
AB EP 399454 A UPAB: 19930928
The device has a substrate (1) of one **conductivity type** (P) and an epitaxial layer (4) formed on it of same conductivity. A charge transfer device section (200) is formed in the epi-layer and a preset region (3-1, 5-1, 6-1) of another **conductivity type** (N) is formed next to the charge transfer section.

The preset layer consists of one layer formed in the boundary between the substrate and epi-layer, another layer in the epi-layer and a third on top to reach the surface of the epi-layer. The maximum impurity concentration of third layer is less than that in the first layer. A bipolar **transistor** section (100) is formed in the third layer.

ADVANTAGE - Enables CCD, bipolar and MOS circuits on single **chip** without degradation of performance or reliability.
1H/6

L41 ANSWER 9 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1990-147423 [19] WPIX
DNN N1990-114227 DNC C1990-064571
TI Vertical power DMOS **transistor** with small signal NPN **transistors** - method may also include CMOS **transistors** and has self-alignment of gate source and channel regions.
DC L03 U13
IN HUIE, W K; OWENS, A H; PAN, D S; ZUNINO, M J
PA (SPRA) SPRAGUE ELECTRIC CO
CYC 1
PI US 4914051 A 19900403 (199019)* <--
ADT US 4914051 A US 1988-281593 19881209
PRAI US 1988-281593 19881209
AB US 4914051 A UPAB: 19930928
A method of making an **IC** combining a high current vertical DMOS **transistor** in one epitaxial pocket (12d) in Si(10) and a small signal vertical NPN **transistor** in a second pocket. Isolation walls define the pockets and free-standing D-**well regions** (16d) are formed in the first pocket and a base in the second pocket. An elemental source region (20d) is formed in each D-well and an emitter in the base region. Heavily doped buried layers (24d) of

the same polarity type as the emitter and source are formed in the pockets respectively.

Two plug regions (26d) extend through the pockets from the buried layers to an outer epitaxial surface. A glass layer (33) is formed on the surface having a hole over a part of each of the elemental DMOS source regions, and a hole over the isolation wall and extending over part of the corresponding D-**well region**. A metal conductor (35) is over the glass layer and through the holes to make contact with the source and D-well and connect the source regions to each other and the isolation wall (22w). This serves as the single source contact. Another hole is formed over the glass layer over the DMOS plug region in the first pocket and a separate metal conductor acts as the DMOS drain contact.

USE/ADVANTAGE - High current capacity vertical DMOS power **transistor** integrated with small signal vertical NPN **transistors** (claimed) is provided. The method is efficient w.r.t. the number of steps and has self-aligned gate, channel and source regions. Small signal CMOS **transistors** may also be provided in the **IC**. The DMOS **transistors** may be used for driving solenoids and other high current loads.
1/6

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L41  ANSWER 10 OF 30  WPIX (C) 2002 THOMSON DERWENT
AN   1990-120423 [16]   WPIX
TI   Semiconductor IC - has bipolar-transistor collectors
     in P-type and N-type regions on conduction-type
     substrate  NoAbstract Dwg 1e,j/5.
DC   U12 U13
PA   (MATU) MATSUSHITA ELEC IND CO LTD
CYC  1
PI   JP 02071526   A  19900312 (199016)*          <--
ADT  JP 02071526 A JP 1988-169405 19880707
PRAI JP 1988-169405    19880707

L41  ANSWER 11 OF 30  WPIX (C) 2002 THOMSON DERWENT
AN   1989-186419 [26]   WPIX
DNN  N1989-142393         DNC C1989-082427
TI   High-voltage bipolar power transistor - is integrated with
     low-voltage MOS power transistor structure in emitter switching
     configuration to combine discrete component  benefits.
DC   L03 U12 U13 U21
IN   FERLA, G; FRISINA, F
PA   (SGSA) SGS MICROELETTRONICA SPA; (SGSA) SGS-THOMSON MICROEL; (SGSA) SGS
     THOMSON MICROELTRN SRL
CYC  8
PI   EP 322041      A  19890628 (198926)* EN    8p <--
         R: DE FR GB NL
     JP 02002665    A  19900108 (199007)           <--
     US 5065213     A  19911112 (199148)        8p <--
     IT 1217323     B  19900322 (199208)           <--
     US 5118635     A  19920602 (199225)        8p <--
     EP 322041      A3 19930421 (199401)           <--
     EP 322041      B1 19961009 (199645)  EN    8p <--
         R: DE FR GB NL
     DE 3855603     G  19961114 (199651)           <--
     US 35642       E  19971028 (199749)        9p <--
     US 36311       E  19990921 (199945)           <--
     KR 130774      B1 19980406 (200009)           <--
ADT  EP 322041 A EP 1988-202899 19881216; JP 02002665 A JP 1988-322215
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19881222; US 5065213 A US 1988-288405 19881221; US 5118635 A Div ex US 1988-288405 19881221, US 1991-749251 19910823; EP 322041 A3 EP 1988-202899 19881216; EP 322041 B1 EP 1988-202899 19881216; DE 3855603 G DE 1988-3855603 19881216, EP 1988-202899 19881216; US 35642 E US 1988-288405 19881221, Cont of US 1993-152959 19931112, US 1995-447184 19950522; US 36311 E Div ex US 1988-288405 19881221, US 1991-749251 19910823, US 1994-253151 19940602; KR 130774 B1 KR 1988-17103 19881221

FDT US 5118635 A Div ex US 5065213; DE 3855603 G Based on EP 322041; US 35642 E Reissue of US 5065213; US 36311 E Div ex US 5065213, Reissue of US 5118635

PRAI IT 1987-6631 19871222

AB EP 322041 A UPAB: 19940217
An integrated structure in the emitter switching configuration comprises a higher voltage bipolar power **transistor** and a low-voltage MOS power **transistor**. In the vertical MOS version, the emitter region of the bipolar **transistor** is completely buried, partly in a first N-epitaxial layer and partly in a second N-epitaxial layer. With the MOS located above the emitter region, the bipolar is thus a completely buried active structure.
USE/ADVANTAGE - Bipolar **transistor** strength is increased w.r.t. inverted secondary rupture occurence. Current/voltage carrying capacity of piloted **transistor** is combined with the high speed of low-voltage **transistor**. The system can be piloted directly with linear **logic circuits** through the MOS gate.
8/12

L41 ANSWER 12 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1988-087479 [13] WPIX
CR 1987-131788 [19]; 1987-163413 [23]; 1987-311276 [44]; 1987-316847 [45]
DNN N1988-065906 DNC C1988-039252
TI Semiconductor **integrated circuit** memory esp. SRAM, with bipolar **transistor** and MISFET - includes increased impurity concn. buried region in substrate, beneath memory cell array, of opposite conductivity to the memory array region, to prevent minority carrier injection from peripheral circuitry bipolar **transistors**.
DC U13 U14
IN HOMMA, N; HORI, R; IKEDA, T; ITOH, K; KITSUKAWA, G; KOBAYASHI, Y; NAKAZATO, S; SAITO, Y; SHIMOHIGASHI, K; TANBA, N; UCHIDA, H; WATANABE, T; YAMAMURA, M
PA (HITA) HITACHI LTD
CYC 3

| | | | | | | |
|---|---|---|---|---|---|---|
| PI | JP 63037651 | A | 19880218 | (198813)* | 21p | <-- |
| | US 5324982 | A | 19940628 | (199426)B | 55p | <-- |
| | US 5386135 | A | 19950131 | (199511) | 54p | <-- |
| | US 5497023 | A | 19960305 | (199615) | 53p | <-- |
| | KR 9510286 | B1 | 19950912 | (199846) | | <-- |

ADT JP 63037651 A JP 1986-179913 19860801; US 5324982 A CIP of US 1986-899405 19860822, CIP of US 1987-29681 19870324, CIP of US 1987-87256 19870713, Cont of US 1988-262030 19881025, Cont of US 1991-645351 19910123, US 1991-769680 19911002; US 5386135 A CIP of US 1986-899405 19860822, CIP of US 1987-29681 19870324, CIP of US 1987-87256 19870713, Cont of US 1988-262030 19881025, Cont of US 1991-645351 19910123, Div ex US 1991-769680 19911002, US 1994-229340 19940412; US 5497023 A CIP of US 1986-899405 19860822, CIP of US 1987-29681 19870324, CIP of US 1987-87256 19870713, Cont of US 1988-262030 19881025, Cont of US 1991-645351 19910123, Div ex US 1991-769680 19911002, Div ex US 1994-229340 19940412, US 1994-352238 19941208; KR 9510286 B1 KR 1987-2628 19870323

FDT US 5324982 A Cont of US 5148255; US 5386135 A Cont of US 5148255, Div ex US 5324982; US 5497023 A Cont of US 5148255, Div ex US 5324982, Div ex US

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     5386135
PRAI JP 1986-179913   19860801; JP 1985-209971   19850925; JP 1985-258506
     19851120; JP 1986-64055    19860324; JP 1986-65696    19860326; WO
     1986-JP579    19861112
AB   US    5324982 A UPAB: 19940817  ABEQ treated as Basic
     device, having structure wherein invasion of minority carriers from the
     semiconductor substrate into components of the device, formed on the
     substrate, can be avoided.
          The semiconductor memory includes a memory array, contg. MOS memory
     cells, and a peripheral circuit, with bipolar transistors, on a
     p-type substrate. There is a p+ buried layer, of the same conductivity as
     the substrate, but with a higher impurity concentration, beneath either or
     both the peripheral circuit and the memory array, pref. beneath the cell
     array. A region extends from the buried layer, e.g. to the substrate
     surface, to act together with the buried layer as a shield to prevent
     minority carriers reaching memory cells.
          There are carrier absorbing n+-regions, an n+-guard ring and an n+
     buried layer, respectively around and beneath input protective elements,
     which are positioned near the peripheral circuit. Pref. the bipolar
     transistors include an npn bipolar transistor having an
     n+-buried layer.
          USE/ADVANTAGE - Also DRAM. Soft error immunity.
     Dwg.18/50

L41  ANSWER 13 OF 30  WPIX (C) 2002 THOMSON DERWENT
AN   1988-051184 [08]    WPIX
DNN  N1988-038878        DNC C1988-022623
TI   CMOS circuit with integrated bipolar transistors - has oxide
     isolation between wells and doped poly crystalline silicon plugs for
     collector controls.
DC   L03 U11 U13
IN   NEPPL, F; WINNERL, J
PA   (SIEI) SIEMENS AG
CYC  8
PI   EP 256315     A  19880224 (198808)* DE    7p <--
         R: DE FR GB IT SE
     JP 63047963   A  19880229 (198814)           <--
     US 4884117    A  19891128 (199006)        4p <--
     CA 1282872    C  19910409 (199131)           <--
     US 5034338    A  19910723 (199132)           <--
     EP 256315     B  19920129 (199205)           <--
         R: DE FR GB IT SE
     DE 3776454    G  19920312 (199212)           <--
ADT  EP 256315 A EP 1987-110230 19870715; JP 63047963 A JP 1987-200764
     19870811; US 4884117 A US 1989-323218 19890315; US 5034338 A US
     1989-379108 19890713; DE 3776454 G DE 1986-3627509 19860813
PRAI DE 1986-3627509  19860813
AB   EP    256315 A UPAB: 19930923
     The integrated circuit contains pref. n-wells (5) in a
     p-type substrate (1) which may have an epitaxial layer of e.g. 3 micron
     thicknessandpref. 20 ohm.cm, but may also be of the opposite type, and
     have p-wells.  The wells are bordered by polycrystalline Si (11) of the
     same conductivity type but higher conductivity which
     also provides the electrical collector-contacts. The moat in which the
     polysi has been deposited has the sides lined with a SiO2 layer (10).
          The moats are etched, after the wells and local oxide layer have been
     formed, by using photolithography and pref. a dry-etch process and have a
     depth equal to the epitaxial layer thickness. Then pref. an oxide layer is
     formed, pref. by deposition, which by anisotropic etching, is removed
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again apart from that adhering to the sidewalls. Doped polycrystalline Si (11) is then deposited to fill the moats. The circuits are then completed in the standard way.

USE/ADVANTAGE - Process restricts sideway diffusion of the wells which allows the wells to be placed closer together, increasing the packing density. The collector capacitance is reduced by avoiding the standard diffused deep contact. The latch-up resistance is also increased. The process is used in the mfr. of VLSI bipolar-CMOS circuits for high operating frequencies.

4/4

L41 ANSWER 14 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1987-316847 [45] WPIX
CR 1987-131788 [19]; 1987-163413 [23]; 1987-311276 [44]; 1988-087479 [13]
DNN N1987-237020 DNC C1987-134891
TI Semiconductor **integrated circuit** memory esp. SRAM, with bipolar **transistor** and MISFET - includes increased impurity concn. buried region in substrate, beneath memory cell array, of opposite conductivity to the memory array region, to prevent minority carrier injection from peripheral circuitry bipolar **transistors**.
DC U13 U14
IN HOMMA, N; HORI, R; IKEDA, T; ITOH, K; KITSUKAWA, G; KOBAYASHI, Y; NAKAZATO, S; SAITO, Y; SHIMOHIGASHI, K; TANBA, N; UCHIDA, H; WATANABE, T; YAMAMURA, M
PA (HITA) HITACHI LTD
CYC 3

| | | | | | | |
|---|---|---|---|---|---|---|
| PI | JP 62224066 | A | 19871002 | (198745)* | 3p | |
| | US 5324982 | A | 19940628 | (199426)B | 55p | <-- |
| | US 5386135 | A | 19950131 | (199511) | 54p | <-- |
| | US 5497023 | A | 19960305 | (199615) | 53p | <-- |
| | KR 9510286 | B1 | 19950912 | (199846) | | <-- |

ADT JP 62224066 A JP 1986-65696 19860326; US 5324982 A CIP of US 1986-899405 19860822, CIP of US 1987-29681 19870324, CIP of US 1987-87256 19870713, Cont of US 1988-262030 19881025, Cont of US 1991-645351 19910123, US 1991-769680 19911002; US 5386135 A CIP of US 1986-899405 19860822, CIP of US 1987-29681 19870324, CIP of US 1987-87256 19870713, Cont of US 1988-262030 19881025, Cont of US 1991-645351 19910123, Div ex US 1991-769680 19911002, US 1994-229340 19940412; US 5497023 A CIP of US 1986-899405 19860822, CIP of US 1987-29681 19870324, CIP of US 1987-87256 19870713, Cont of US 1988-262030 19881025, Cont of US 1991-645351 19910123, Div ex US 1991-769680 19911002, Div ex US 1994-229340 19940412, US 1994-352238 19941208; KR 9510286 B1 KR 1987-2628 19870323
FDT US 5324982 A Cont of US 5148255; US 5386135 A Cont of US 5148255, Div ex US 5324982; US 5497023 A Cont of US 5148255, Div ex US 5324982, Div ex US 5386135
PRAI JP 1986-65696 19860326; JP 1985-209971 19850925; JP 1985-258506 19851120; JP 1986-64055 19860324; JP 1986-179913 19860801; WO 1986-JP579 19861112
AB US 5324982 A UPAB: 19940817 ABEQ treated as Basic device, having structure wherein invasion of minority carriers from the semiconductor substrate into components of the device, formed on the substrate, can be avoided.

The semiconductor memory includes a memory array, contg. MOS memory cells, and a peripheral circuit, with bipolar **transistors**, on a p-type substrate. There is a p+ buried layer, of the same conductivity as the substrate, but with a higher impurity concentration, beneath either or both the peripheral circuit and the memory array, pref. beneath the cell array. A region extends from the buried layer, e.g. to the substrate surface, to act together with the buried layer as a shield to prevent

minority carriers reaching memory cells.
There are carrier absorbing n+-regions, an n+-guard ring and an n+ buried layer, respectively around and beneath input protective elements, which are positioned near the peripheral circuit. Pref. the bipolar **transistors** include an npn bipolar **transistor** having an n+-buried layer.
USE/ADVANTAGE - Also DRAM. Soft error immunity.
Dwg.18/50

L41 ANSWER 15 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1987-311276 [44] WPIX
CR 1987-131788 [19]; 1987-163413 [23]; 1987-316847 [45]; 1988-087479 [13]
DNN N1987-232917 DNC C1987-132610
TI Semiconductor **integrated circuit** memory esp. SRAM, with bipolar **transistor** and MISFET - includes increased impurity concn. buried region in substrate, beneath memory cell array, of opposite conductivity to the memory array region, to prevent minority carrier injection from peripheral circuitry bipolar **transistors**.
DC U13 U14
IN HOMMA, N; HORI, R; IKEDA, T; ITOH, K; KITSUKAWA, G; KOBAYASHI, Y; NAKAZATO, S; SAITO, Y; SHIMOHIGASHI, K; TANBA, N; UCHIDA, H; WATANABE, T; YAMAMURA, M
PA (HITA) HITACHI LTD
CYC 3

| | | | | | | |
|---|---|---|---|---|---|---|
| PI | JP 62221145 | A | 19870929 | (198744)* | 54p | |
| | US 5324982 | A | 19940628 | (199426)B | 55p | <-- |
| | US 5386135 | A | 19950131 | (199511) | 54p | <-- |
| | US 5497023 | A | 19960305 | (199615) | 53p | <-- |
| | KR 9510286 | B1 | 19950912 | (199846) | | <-- |

ADT JP 62221145 A JP 1986-64055 19860324; US 5324982 A CIP of US 1986-899405 19860822, CIP of US 1987-29681 19870324, CIP of US 1987-87256 19870713, Cont of US 1988-262030 19881025, Cont of US 1991-645351 19910123, US 1991-769680 19911002; US 5386135 A CIP of US 1986-899405 19860822, CIP of US 1987-29681 19870324, CIP of US 1987-87256 19870713, Cont of US 1988-262030 19881025, Cont of US 1991-645351 19910123, Div ex US 1991-769680 19911002, US 1994-229340 19940412; US 5497023 A CIP of US 1986-899405 19860822, CIP of US 1987-29681 19870324, CIP of US 1987-87256 19870713, Cont of US 1988-262030 19881025, Cont of US 1991-645351 19910123, Div ex US 1991-769680 19911002, Div ex US 1994-229340 19940412, US 1994-352238 19941208; KR 9510286 B1 KR 1987-2628 19870323
FDT US 5324982 A Cont of US 5148255; US 5386135 A Cont of US 5148255, Div ex US 5324982; US 5497023 A Cont of US 5148255, Div ex US 5324982, Div ex US 5386135
PRAI JP 1986-64055 19860324; JP 1985-209971 19850925; JP 1985-258506 19851120; JP 1986-65696 19860326; JP 1986-179913 19860801; WO 1986-JP579 19861112
AB US 5324982 A UPAB: 19940817 ABEQ treated as Basic device, having structure wherein invasion of minority carriers from the semiconductor substrate into components of the device, formed on the substrate, can be avoided.
The semiconductor memory includes a memory array, contg. MOS memory cells, and a peripheral circuit, with bipolar **transistors**, on a p-type substrate. There is a p+ buried layer, of the same conductivity as the substrate, but with a higher impurity concentration, beneath either or both the peripheral circuit and the memory array, pref. beneath the cell array. A region extends from the buried layer, e.g. to the substrate surface, to act together with the buried layer as a shield to prevent minority carriers reaching memory cells.
There are carrier absorbing n+-regions, an n+-guard ring and an n+

buried layer, respectively around and beneath input protective elements, which are positioned near the peripheral circuit. Pref. the bipolar **transistors** include an npn bipolar **transistor** having an n+-buried layer.
USE/ADVANTAGE - Also DRAM. Soft error immunity.
Dwg.18/50

L41 ANSWER 16 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1987-235180 [33] WPIX
DNN N1987-175942
TI High current lateral **transistor** structure for **IC** - has base contacts shorting together second and base regions to prevent excess current during saturation.
DC U12
IN SIKINA, T V; SLOANE, M W
PA (RADC) RCA CORP
CYC 1
PI US 4684970 A 19870804 (198733)* 5p <--
ADT US 4684970 A US 1986-885744 19860721
PRAI US 1985-759831 19850729; US 1986-885744 19860721
AB US 4684970 A UPAB: 19930922
The **transistor** includes a substrate of a first **conductivity type** semiconducting material. A layer of second **conductivity type** semiconducting material having a surface is positioned on the substrate. The layer has a thickness extending from the surface to the substrate. A region of highly doped first **conductivity type** is disposed within and in PN junction forming relation with the layer and extends downwardly from the surface for a distance equal to a portion of the thickness.
A second region of highly doped first **conductivity type** is positioned within and in PN junction forming relation with the layer. The second region is spaced from and surrounds the first region and extends downwardly from the surface for a distance equal to the portion of the thickness. A third region of highly doped first **conductivity type** is positioned within and in PN junction forming relation with the layer. The third region is spaced from and surrounds the second region and extends downwardly from the surface.
1/3

L41 ANSWER 17 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1987-163413 [23] WPIX
CR 1987-131788 [19]; 1987-311276 [44]; 1987-316847 [45]; 1988-087479 [13]
DNN N1994-164504
TI Semiconductor **integrated circuit** memory esp. SRAM, with bipolar **transistor** and MISFET - includes increased impurity concn. buried region in substrate, beneath memory cell array, of opposite conductivity to the memory array region, to prevent minority carrier injection from peripheral circuitry bipolar **transistors**.
DC U13 U14
IN HOMMA, N; HORI, R; IKEDA, T; ITOH, K; KITSUKAWA, G; KOBAYASHI, Y; NAKAZATO, S; SAITO, Y; SHIMOHIGASHI, K; TANBA, N; UCHIDA, H; WATANABE, T; YAMAMURA, M
PA (HITA) HITACHI LTD; (KITS-I) KITSUKAWA G
CYC 7
PI WO 8703423 A 19870604 (198723)* JA 39p <--
RW: DE FR GB
W: KR US
JP 62119958 A 19870601 (198727) <--
EP 245515 A 19871119 (198746) EN <--

R: DE FR GB
US 5148255 A 19920915 (199240) 56p <--

AB US 5324982 A UPAB: 19940817 ABEQ treated as Basic
device, having structure wherein invasion of minority carriers from the semiconductor substrate into components of the device, formed on the substrate, can be avoided.

The semiconductor memory includes a memory array, contg. MOS memory cells, and a peripheral circuit, with bipolar **transistors**, on a p-type substrate. There is a p+ buried layer, of the same conductivity as the substrate, but with a higher impurity concentration, beneath either or both the peripheral circuit and the memory array, pref. beneath the cell array. A region extends from the buried layer, e.g. to the substrate surface, to act together with the buried layer as a shield to prevent minority carriers reaching memory cells.

There are carrier absorbing n+-regions, an n+-guard ring and an n+ buried layer, respectively around and beneath input protective elements, which are positioned near the peripheral circuit. Pref. the bipolar **transistors** include an npn bipolar **transistor** having an n+-buried layer.

L41 ANSWER 18 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1987-131788 [19] WPIX
CR 1987-163413 [23]; 1987-311276 [44]; 1987-316847 [45]; 1988-087479 [13]
DNN N1987-098429 DNC C1987-054711
TI Semiconductor **integrated circuit** memory esp. SRAM, with bipolar **transistor** and MISFET - includes increased impurity concn. buried region in substrate, beneath memory cell array, of opposite conductivity to the memory array region, to prevent minority carrier injection from peripheral circuitry bipolar **transistors**.
DC U13 U14
IN HOMMA, N; HORI, R; IKEDA, T; ITOH, K; KITSUKAWA, G; KOBAYASHI, Y; NAKAZATO, S; SAITO, Y; SHIMOHIGASHI, K; TANBA, N; UCHIDA, H; WATANABE, T; YAMAMURA, M
PA (HITA) HITACHI LTD
CYC 2
PI JP 62071265 A 19870401 (198719)* 5p
US 5324982 A 19940628 (199426)B 55p <--
US 4409606 A 19831011 (198343)

AB US 5324982 A UPAB: 19940817 ABEQ treated as Basic
device, having structure wherein invasion of minority carriers from the semiconductor substrate into components of the device, formed on the substrate, can be avoided.

The semiconductor memory includes a memory array, contg. MOS memory cells, and a peripheral circuit, with bipolar **transistors**, on a p-type substrate. There is a p+ buried layer, of the same conductivity as the substrate, but with a higher impurity concentration, beneath either or both the peripheral circuit and the memory array, pref. beneath the cell array. A region extends from the buried layer, e.g. to the substrate surface, to act together with the buried layer as a shield to prevent minority carriers reaching memory cells.

There are carrier absorbing n+-regions, an n+-guard ring and an n+ buried layer, respectively around and beneath input protective elements, which are positioned near the peripheral circuit. Pref. the bipolar **transistors** include an npn bipolar **transistor** having an n+-buried layer.

USE/ADVANTAGE - Also DRAM. Soft error immunity.
Dwg.18/50

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L41  ANSWER 19 OF 30  WPIX (C) 2002 THOMSON DERWENT
AN   1987-088128 [13]   WPIX
DNN  N1987-066125        DNC C1987-036526
TI   Bipolar integrated circuit - has oxide isolation and
     substrate contacts.
DC   L03 U11 U12
IN   HUA, T C; LAWRENCE, Y; SCOTT, O G; LAWRENCE, Y C L; LAWRENCE, Y L
PA   (MONO-N) MONOLITHIC MEMORIES INC; (ADMI) ADVANCED MICRO DEVICES INC
CYC  6
PI   EP 216435      A   19870401 (198713)* EN    13p <--
         R: DE FR GB NL
     US 4721682     A   19880126 (198807)         5p <--
     JP 63023335    A   19880130 (198810)            <--
     EP 216435      B1 19930317 (199311)  EN     7p <--
         R: DE FR GB NL
     DE 3688030     G   19930422 (199317)            <--
ADT  EP 216435 A EP 1986-201651 19860924; US 4721682 A US 1985-780062 19850925;
     JP 63023335 A JP 1986-225049 19860925; EP 216435 B1 EP 1986-201651
     19860924; DE 3688030 G DE 1986-3688030 19860924, EP 1986-201651 19860924
FDT  DE 3688030 G Based on EP 216435
PRAI US 1985-780062     19850925
AB   EP     216435 A UPAB: 19930922
     The integrated circuit, fig 1a, is built up from a
     p-type semiconductor substrate (102), pref. single crystalline Si, on
     which an epitaxial layer (104) has been deposited. In the epitaxial layer
     regions in which a transistor is formed, are isolated laterally
     by surrounding insulating regions (108,110) pref. made of Si-oxide, which
     extend from the layer-surface to the substrate-surface. Within the regions
     isolated in this way a base (100b) and an emitter-layer (100e) may be mfd.
     to form a vertical npn-transistor.
          Sepg. the isolated regions is a p+-type conductive region which
     extends from the surface of the epitaxial layer to the surface of the
     substrate and allows electrical contact to be made to the substrate. The
     structure may also have an n+-type buried layer (106) in the substrate,
     aligned with the isolated region, to which electrical contact can be made
     within the isolated region by an n+-diffusion. This forms a collector
     electrical contact.
          USE/ADVANTAGE - The insulating Si-oxide allows a diffused contact to
     be made to the buried layer and to the substrate. The base to collector
     capacitance is not increased by this. The process is simpler than current
     art and requires only a small surface area.
     1a/2

L41  ANSWER 20 OF 30  WPIX (C) 2002 THOMSON DERWENT
AN   1984-083375 [14]   WPIX
DNN  N1984-062231        DNC C1984-035354
TI   Integrated semiconductor device prodn. - esp. IC with bipolar
     transistor and MOSFET with high integration density.
DC   L03 U11 U13
IN   ANZAI, N; YASUOKA, H
PA   (HITA) HITACHI LTD
CYC  9
PI   DE 3334337     A   19840329 (198414)*       32p <--
     GB 2128024     A   19840418 (198416)            <--
     FR 2533751     A   19840330 (198418)            <--
     JP 59055052    A   19840329 (198419)            <--
     US 4529456     A   19850716 (198531)            <--
     GB 2128024     B   19860102 (198601)            <--
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     IT 1168294     B  19870520 (198942)           <--
     JP 04081337    B  19921222 (199303)        6p <--
     KR 9201403     B1 19920213 (199342)           <--
ADT  DE 3334337 A DE 1983-3334337 19830922; GB 2128024 A GB 1983-24163
     19830909; FR 2533751 A FR 1983-9953 19830616; JP 59055052 A JP 1982-164840
     19820924; US 4529456 A US 1983-531708 19830913; GB 2128024 B GB 1983-24163
     19830709; JP 04081337 B JP 1982-164840 19820924; KR 9201403 B1 KR
     1983-3011 19830701
FDT  JP 04081337 B Based on JP 59055052
PRAI JP 1982-164840    19820924
AB   DE    3334337 A UPAB: 19930925
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Process involves (1) introducing an impurity of a first **conductivity type** into a number of pts. of the surface of a substrate contg. an impurity of the first **conductivity type** to form more highly doped zones; (2) producing an epitaxial semiconductor film contg. an impurity of the second **conductivity type** on the surface; (3) introducing an impurity of the first **conductivity type** into the epitaxial layer over the numerous doped zones; (4) introducing the impurity of the first **conductivity type** into the epitaxial film by forced diffusion from the doped zones in the substrate and on the surface of the epitaxial film to connect the diffusion layers and produce an insulation zone and a semiconductor zone, giving a MOSFET; (5) producing a thick oxide film on the surface of the insulating zone; (6) forming the MOSFET in the semiconductor zone; and (7) forming a bipolar **transistor** in pt. of the epitaxial film. The process is useful for the prodn. of Bi-MOSICs with bipolar **transistors** and MOSFETs in the same device. It is rapid and gives high integration density.
0/24

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L41  ANSWER 21 OF 30  WPIX (C) 2002 THOMSON DERWENT
AN   1983-47221K [20]   WPIX
DNN  N1983-085065        DNC C1983-045814
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TI **IC** contg. bipolar **transistor** and pref. igfets - is formed using buried layers to diffuse second type islands and first type regions.

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DC   L03 U11 U13
IN   JOCHEMS, P J W
PA   (PHIG) PHILIPS GLOEILAMPENFAB NV
CYC  11
PI   EP 78571       A  19830511 (198320)* EN   20p <--
         R: CH DE FR GB IT LI NL
     NL 8104862     A  19830516 (198323)           <--
     AU 8289763     A  19830505 (198325)           <--
     JP 58080851    A  19830516 (198325)           <--
     EP 78571       B  19850703 (198527)  EN       <--
         R: CH DE FR GB IT LI NL
     DE 3264580     G  19850808 (198533)           <--
     CA 1203639     A  19860422 (198620)           <--
     US 4724221     A  19880209 (198809)           <--
     JP 04363046    A  19921215 (199304)        8p <--
ADT  EP 78571 A EP 1982-201335 19821026; US 4724221 A US 1986-883008 19860707;
     JP 04363046 A Div ex JP 1982-186217 19821025, JP 1991-240286 19821025
PRAI NL 1981-4862       19811028
AB   EP     78571 A UPAB: 19930925
```

An **IC** comprises (a) a first **conductivity type** substrate (1); (b) an epitaxial layer (2) divided into second type islands (2A,2B) laterally surrounded by first type regions, formed by adjoining regions diffused through the layer from adjacent buried first-and

second-type layers at the interface between substrate and layer, the pn junctions (4A, 4B) between islands and surrounding regions being at right angles to the layer surface; (c) a bipolar **transistor** in at least one island (2B) and pref. (d) an IGFET in another island (2A) and esp. (e) a complementary IGFET in a surrounding region.

The device is made by (i) providing second-type islands in a first type substrate surface by doping through an apertured mask; (ii) providing first type dopant in the whole region between islands to form a surface layer of higher first-type dopant concn. than the substrate; (iii) growing an undoped epitaxial layer on the surface; (iv) diffusing dopants through the whole thickness of the epitaxial layer; and (v) forming a bipolar **transistor** in a second type island.

A compact structure is provided, with high speed bipolar **transistors**, having low dissipation. FETs are included without problems and bipolar and MOS **transistors** can be independently optimised.

1/12

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L41  ANSWER 22 OF 30  WPIX (C) 2002 THOMSON DERWENT
AN   1981-J7884D [38]   WPIX
TI   Zone arrangement for semiconductor device e.g. transistor - has
     separation region extending through semiconductor layer and surrounding
     island-region providing high break down voltage.
DC   U12
IN   AAR, K J W; APPELS, J A; DEGRAAFF, H C
PA   (PHIG) PHILIPS GLOEILAMPENFAB NV
CYC  8
PI   GB 2071412    A  19810916 (198138)*      9p <--
     DE 3047738    A  19810924 (198140)          <--
     FR 2477776    A  19810911 (198142)          <--
     NL 8001409    A  19811001 (198144)          <--
     SE 8009091    A  19811012 (198144)          <--
     US 4409606    A  19831011 (198343)          <--
     CA 1155971    A  19831025 (198347)          <--
     GB 2071412    B  19840418 (198416)          <--
     DE 3047738    C  19860717 (198629)          <--
     NL 186665     B  19900816 (199035)          <--
     IT 1194011    B  19880831 (199106)          <--
ADT  DE 3047738 A DE 1980-3047738 19801218; NL 186665 B NL 1980-1409 19800310
PRAI NL 1980-1409     19800310
AB   GB    2071412 A UPAB: 19930915
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The semiconductor device (e.g. a bipolar or field-effect **transistor**) has an n-type layer (3) on a p-type substrate (4). Present within an island-shaped region (3A) of the layer (3) are a surface-adjoining p-type active zone (8) (e.g. the base of a bipolar **transistor** or the channel of a field effect **transistor**) and a juxtaposed highly doped n-type contact zone (9). The thickness and the doping concentration of the layer (3) are so small that the layer is depleted up to the surface (2) at a reverse voltage across the p-n junction (5) which is lower than the breakdown voltage.

To minimise lateral current concentrations (i.e. Kirk effect) while maintaining a high breakdown voltage a highly doped n-type buried layer (11) is present between layer (3) and substrate (4). The layer (11) extends below at least a portion of the active zone (8).

```
L41  ANSWER 23 OF 30  WPIX (C) 2002 THOMSON DERWENT
AN   1980-D9392C [18]   WPIX
CR   1983-E0599K [12]
TI   Power MOS FET system structure - uses high blocking voltage and has low
```

switching resistance attained by common region of relatively higher conductivity (NL 15.4.80).
DC U12
IN HERMAN, T; LIDOW, A; RUMENNIK, V
PA (INRC) INT RECTIFIER CORP; (LIDO-I) LIDOW A; (HERM-I) HERMAN T
CYC 16
PI DE 2940699 A 19800424 (198018)* <--
NL 7907472 A 19800415 (198018) <--
GB 2033658 A 19800521 (198021) <--
DK 7903506 A 19800512 (198023) <--

AB DE 2940699 A UPAB: 19980610
The high power MOSFET includes a semiconductor **wafer** having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of one **conductivity type**.
At least two spaced base regions of opposite conductivity are formed in **wafer** to a first depth. The space between the base regions defines a common conduction region at a given first semiconductor surface location. Two source regions are formed in each pair of the base regions, and are laterally spaced along the first semiconductor surface to define two channel regions, and are connected to respective electrodes. A gate insulation layer is disposed at least on the two channel regions. A drain conductive region is sepd. from the common region by the relatively lightly doped major body portion.

The common region is relatively highly doped, and extends from the given first semiconductor surface location to a depth greater than the depth of the source region. The resistance to current flow at the junctions between the channel regions and the common region and between the common region and the relatively lightly doped major body portion is reduced.

ADVANTAGE - Epitaxially deposited semiconductor material immediately adjacent and beneath the gate and in source-drain path has relatively high conductivity, reducing on-resistance without effecting breakdown voltage. Impurities for defining source regions are applied in single step.

L41 ANSWER 24 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1979-C4681B [11] WPIX
TI Semiconductor **integrated circuit** device - has complementary MOS **transistors** formed in n-type semiconductor substrate formed with p-type **well region**.
DC U12 U13
IN SHIGEMATSU, T; SUZUKI, Y
PA (TOKE) TOKYO SHIBAURA ELECTRIC CO
CYC 2
PI US 4143391 A 19790306 (197911)* <--
GB 1542481 A 19790321 (197912) <--
PRAI JP 1975-109940 19750912
AB US 4143391 A UPAB: 19940205
The **integrated circuit** device comprises a semiconductor substrate in one area of which there is formed a main-**well region** having a **conductivity type** opposite to that of the semiconductor substrate. Complementary MOS circuit elements are formed in the one area of the semiconductor substrate and the main-**well region**, respectively.

Load elements being connected to an input terminal are formed in the other area of the semiconductor substrate excluding the one region having the complementary circuit elements formed therein. At least one of the semiconductor regions constituting those load elements, respectively is formed in an additional region of the opposite condictivity type to that

of the semiconductor substrate, formed in the other region of the semiconductor substrate.

L41 ANSWER 25 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1979-C3061B [11] WPIX
TI Semiconductor **integrated circuit** - includes back gate type junction field effect and bipolar **transistors** with integrated resistor.
DC U12 U13
IN KOMEDA, T; TAKEMOTO, T; YAMADA, H
PA (MATU) MATSUSHITA ELEC IND CO LTD
CYC 4

| | | | | | |
|---|---|---|---|---|---|
| PI | GB 2003661 | A | 19790314 | (197911)* | <-- |
| | DE 2837028 | A | 19790315 | (197912) | <-- |
| | US 4233615 | A | 19801111 | (198048) | <-- |
| | CA 1121518 | A | 19820406 | (198217) | <-- |
| | GB 2003661 | B | 19820519 | (198220) | <-- |
| | DE 2837028 | C | 19880922 | (198838) | <-- |

PRAI JP 1977-102427 19770825
AB GB 2003661 A UPAB: 19940205
An **IC** in a semiconductor substrate includes a junction gate FET including a gate region in which source and drain regions are formed of opposite **conductivity type** to the gate region. A surface channel region has a lower resistivity and is shallower than the source and drain regions and connects these regions together.
A doped surface region has a higher impurity concentration and a shallower depth than the channel region and is formed in the channle spaced from the source and drain regions. The circuit may also inlude a vertical bipolar **transistor** and a resistor.

L41 ANSWER 26 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1978-E6592A [24] WPIX
TI Structure for digital **integrated circuit** - has two **transistors** of one **conduction type** and one **transistor** of other type enclosed in insulating trough.
DC U12 U13 U21 U22
IN NUZILLAT, G
PA (CSFC) THOMSON CSF
CYC 5

| | | | | | |
|---|---|---|---|---|---|
| PI | DE 2753882 | A | 19780608 | (197824)* | <-- |
| | FR 2373163 | A | 19780804 | (197836) | <-- |
| | GB 1585929 | A | 19810311 | (198111) | <-- |
| | US 4277794 | A | 19810707 | (198130) | <-- |
| | CA 1113614 | A | 19811201 | (198201) | <-- |
| | DE 2753882 | C | 19820204 | (198206) | <-- |

PRAI FR 1976-36534 19761203
AB DE 2753882 C UPAB: 19930901
The digital, **integrated circuit** contains in the same semiconductor substrate a first p-n-p or n-p-n **transistor** connected as a current source, with its base and emitter connected to two fixed bias voltage sources; a second **transistor** of the same type and a third **transistor** of a complementary type. The second and third **transistor** form an alternating series of junctions.
The second and third **transistors** are vertical **transistors** and are enclosed in an insulating trough forming a junction with the substrate. A first part of the trough serves as first **transistor** collector, and its second part as the second **transistor** emitter.

L41 ANSWER 27 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1975-86277W [52] WPIX
TI Making a semiconductor having a buried epitaxial layer - comprises growing an epitaxial layer in a recess of the semiconductor and diffusing impurity into a closed loop.
DC L03 U11 U12
PA (HITA) HITACHI LTD
CYC 1
PI US 3925120 A 19751209 (197552)* <--
PRAI JP 1969-85231 19691027; JP 1970-20884 19700313
AB US 3925120 A UPAB: 19930831
A semiconductor device is made by growing an epitaxial layer of opposite **conductivity type** in a recess in a semiconductor substrate to form an embedded layer coplanar with the substrate and then diffusing an impurity into a closed loop-region extending over the edge of the junction between the substrate and embedded layer and also to the surface of the substrate and the embedded layer. The method is used in the prodn. of an MOS type **integrated circuit**. Islands with high specific resistance can be formed on any desired region with improved junction characteristics. The diffused layer also acts as a channel stopper of a MOS **transistor** and has excellent electrical and noise characteristics.

L41 ANSWER 28 OF 30 WPIX (C) 2002 THOMSON DERWENT
AN 1975-39020W [23] WPIX
TI **Integrated circuit** contg. different devices - having low resistivity regions for high gain **transistors** and controlled valve resistors.
DC L03 U11 U12 U13
PA (ATES-N) ATES COMPONENT ELET
CYC 4
PI US 3885999 A 19750527 (197523)* <--
GB 1403012 A 19750813 (197533) <--
JP 48066978 A 19730913 (197828) <--
JP 53019395 B 19780620 (197828) <--
DE 2261541 B 19780914 (197838) <--
PRAI IT 1971-32459 19711215
AB US 3885999 A UPAB: 19930831
Integrated circuitry contg. several juxtaposed units is made by (a) forming a number of spaced highly doped second-**conductivity-type** (pref. N) strata in a first-**conductivity-type** (pref. P) substrate, (b) growing a less highly doped second-type epitaxial layer to embed the strata, (c) diffusing first-type dopant into the layer through windows in an overlying Si oxide film, to start a downward growth of barriers between sections of the layer contg. the strata, (d) diffusing a high concn. of second-type dopant through another window to form a web unitary with the strata and simultaneously completing barrier growth to contact the substrate and isolate the sections, (e) doping selected surface areas of the sections with a high concn. of first-type dopant through additional windows, (f) introducing a lower concn. of first type dopant through the additional windows, (g) broadening an additional window in a section adjacent th eweb and introducing some of the lower conc. first-type dopant to form a stepped enclave, (h) simultaneously diffusing the impurities form steps (e) and (f) to a predetermined depth and (i) applying metal terminals to selected surface areas.

L41 ANSWER 29 OF 30 JAPIO COPYRIGHT 2002 JPO
AN 1990-137262 JAPIO

TI SEMICONDUCTOR **INTEGRATED CIRCUIT** AND ITS MANUFACTURE
IN OKODA TOSHIYUKI
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
PI **JP 02137262** A 19900525 Heisei
AI JP1988-291448 (JP63291448 Heisei) 19881117
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 964, Vol. 14, No. 374, P. 159 (19900813)
AB PURPOSE: To isolate a **well region** from a substrate, and make it possible to apply a back gate voltage different from a substrate voltage by forming an N+ type buried layer on a semiconductor substrate and an epitaxial layer, and forming a P+ type buried layer between the N+ type buried layer and a P-type **well region**.
CONSTITUTION: A third buried layer 18 is formed in the forming regions of a P-channel type MOS **transistor** 23 and an N-channel type MOS **transistor** 21, which buried layer is arranged between a semiconductor substrate 2 and an epitaxial layer 3. A fourth buried layer 19 of P+ type is formed on a part of the third buried layer 18, so as to be in contact with the third buried layer 18. A P-type **well region** 20 is formed so as to be in contact with the fourth buried layer 19. The first MOS **transistor** 21 of N-channel type is formed in the **well region** 20. Thereby, the third buried layer 18 is isolated from a voltage of the semiconductor substrate 2, so that a back gate voltage different from the substrate voltage can be applied to the N-channel type MOS **transistor** 21.

L41 ANSWER 30 OF 30 JAPIO COPYRIGHT 2002 JPO
AN 1990-071526 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT** AND MANUFACTURE THEREOF
IN YONEDA TADANAKA
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI **JP 02071526** A 19900312 Heisei
AI JP1988-169405 (JP63169405 Heisei) 19880707
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 933, Vol. 14, No. 248, P. 146 (19900528)
AB PURPOSE: To make it possible to isolate between a collector and a substrate without lowering withstand voltage and also without increasing the thickness of an epitaxial layer by a method wherein a one-**conductivity type** region and a first opposite **conductivity type** region are formed successively on the surface of the prescribed region of a one-**conductivity type** substrate, a second opposite **conductivity type** region is formed on the other prescribed region, and an opposite **conductivity type** epitaxial layer is formed on the surface of the substrate.
CONSTITUTION: An SiO2 film 30 is formed on a p-type substrate 29, and injection windows 31 and 32 are formed. Then, injection regions 33 and 34 are formed by injecting ions. Subsequently, an arsenic implantation region 35 is formed by implanting arsenic into silicon from the injection window 32 provided on the region where an n-p-n **transistor** is formed. Then, n-type regions 36 and 37 are formed on the phosphorus-implantation regions 33 and 34 by conducting a prescribed heat treatment. Also, an n-type region 38 is formed on the arsenic-ion implantation region 35. Then, boron implanting windows 39 and 40 are formed using photolithographic technique, boron is ion-implanted and boron-implanted regions 41 and 42 are formed. Subsequently, p+ buried regions 43 and 44 are formed on the boron-implanted regions 41 and 42. Then, an n-type epitaxial layer 45 is formed thereon. As a result, high withstand voltage can be obtained on the

collector 38 and the substrate.

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     FILE 'INSPEC, HCAPLUS' ENTERED AT 10:07:36 ON 08 JUL 2002
L1       455369 S IC OR ICS OR INTEGRATED(W)CIRCUIT OR (MICRO)(W)(CIRCUIT OR CH
L2        71918 S B2570/CC
L3        60382 S (H01L-023 OR H01L-025 OR H01L-029)/IC
L4       175178 S TRANSISTOR
L5        11238 S CONDUCT?(W)TYPE
L6         1587 S WELL(W)(REGION OR AREA OR ZONE)
L7         8793 S (DOPED OR DOPING)(2N)(REGION OR ZONE OR AREA)
L8          306 S CONTACT(W)DIFFUSION
L9        84183 S ION(W)IMPLANT######
L10       89766 S EPITAXIAL(W)(LAYER OR FILM OR COAT####)
L11      513755 S L1-3
L12          71 S L11 AND L8
L13          33 S L12 AND L4
L14           1 S L13 AND L6
L15           1 S L13 AND L7
L16           6 S L13 AND L5
L17           4 S L13 AND L9
L18           7 S L13 AND L10
L19          14 S L14-L18
L20          14 DUP REMOVE L19 (0 DUPLICATES REMOVED)
L21          19 S L13 NOT L20
L22          18 DUP REMOVE L21 (1 DUPLICATE REMOVED)
L23       66089 S L11 AND L4
L24        2599 S L23 AND L5
L25        5156 S BURIED(W)(LAYER OR FILM OR COAT####)
L26         336 S L24 AND L7
L27          22 S L26 AND L6
L28          35 S L26 AND L10
L29          31 S L28 NOT (L13 OR L27)
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L19 ANSWER 1 OF 14 INSPEC COPYRIGHT 2002 IEE
AN 1971:230558 INSPEC DN A71015951; B71006949
TI Polycrystalline silicon technology for bipolar **integrated circuits**.
AU Schoeff, J.A. (Motorola, Mesa, AZ, USA)
SO International electron devices metering (abstracts)
New York, NY, USA: IEEE, 1970. p.74, 6 of 163 pp.
Conference: Washington, DC, USA, 28-30 Oct 1970
Sponsor(s): IEEE, Electron Devices Group
DT Conference Article
CY United States
LA English
AB Abstract only given substantially as follows. Polycrystalline isolation eliminates the standard isolation diffusion and most buried- layer outdiffusion, resulting in thinner epi layers and smaller device islands. A new method of doping the polycrystalline material yields higher breakdown voltages than possible with similar diffusion-isolated **epitaxial layers**, while contributing negligible sidewall capacitance. Nucleation for the isolation channels begins on a thin layer of silicon deposited on a doped-oxide pattern, enabling surfaces free of sharp grains with smooth transitions from channel to device island. Growth takes place with either silane or silicon tetrachloride in conventional epitaxial equipment on both (100) and (111) substrates. A deep collector contact for **IC transistors** can be obtained using only one photoresist step and no special diffusions. Although this contact is the same size as the small shallow collector **contact diffusion** of low-power devices, the polycrystalline contact resistance is lower than that of larger deep n+ diffusions driven down to the buried layer. A single thin polycrystalline silicon film can form collector-base and emitter- base field plates, capacitors, crossunders, and electrostatic shields. This film, particularly when deposited during the epi growth, is easier to process than a second layer of aluminium metallization.

L19 ANSWER 2 OF 14 INSPEC COPYRIGHT 2002 IEE
AN 1969:43890 INSPEC DN B69013484
TI Self-isolated bipolar **transistors** in **integrated circuits**.
AU Makimoto, T.; Maki, M. (Hitachi, Ltd., Central Research Lab., Kokubunji, Tokyo, Japan); Sugawara, K.
SO International electron devices meeting
New York, NY, USA: IEEE, 1968. p.20 of 153 pp.
Conference: Washington, DC, USA, 23-25 Oct 1968
Sponsor(s): IEEE Electron Devices Group
DT Conference Article
CY United States
LA English
AB Abstract only given, substantially as follows: A p-type **epitaxial layer** is grown on a p-type substrate where localized n+-layers are buried, and there is no need for additional isolation diffusion besides n+-collector **contact diffusion**. The higher packing density and the simplicity in processing resulting from the above structures are desirable features for LSI. There are three basic structures, namely, uniform base, selectively graded base, and nonselectively graded base structures. With the uniform base structure, fT of 400 MHz, beta of 100, Rcs of 10 ohms were observed. With the second structure, fT of 600 MHz, beta of 50, and Rcs of 10 ohms were observed. Current and voltage dependences of the major electrical parameters will

be presented. The feasibility of the proposed method should be quite clear from the experimental results. An attractive way of achieving the above structures, which makes use of the simultaneous diffusion of P, As, and Ga, will be discussed. This method will result in further simplification of the processing.

L19 ANSWER 3 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:762401 HCAPLUS
DN 135:312176
TI Fabrication of BiCMOS semiconductor devices for decreased collector resistance without **epitaxial layer** formation
IN Tsujimoto, Koichi
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 2001291781 | A2 | 20011019 | JP 2000-106198 | 20000407 |

AB The title fabrication involves (1) providing a 1st **cond.-type** channel on a 1st **cond.-type** semiconductor substrate, (2) simultaneously forming a 2nd **cond.-type** 1st well for the MOS **transistor** and a 2nd **cond.-type** 2nd well as a collector region for the vertical bipolar **transistor**, and (3) simultaneously forming a 2nd **cond.-type** 1st diffusion regions directly below the MOS **transistor** source/drain/channel regions in the 1st well and also a highly-doped and shallower-depth 2nd **cond.-type** 2nd diffusion regions directly below an ohmic **contact diffusion** region in the bipolar **transistor** collector region. The process provides the npn-type bipolar **transistor** with an increased collector concn. for improving the elec. characteristics without formation of an **epitaxial layer**.

L19 ANSWER 4 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:470107 HCAPLUS
TI Semiconductor device and its production method. [Machine Translation].
IN Goto, Hiroyoshi
PA Nec Ic Microcomputer System, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 2001177061 | A2 | 20010629 | JP 1999-357055 | 19991216 |

AB [Machine Translation of Descriptors]. The formation tries to be able to designate the capacity component of the large capacity which is necessary for the semiconductor device effectively as inside the semiconductor **chip**, in the semiconductor device in high density to be able to load together memory circuit, **logic circuit** or analog circuit try. Well layer 2 and 3 the formation is done on the semiconductor substrate (silicon substrate 1) surface in the semiconductor device which is formed with the semiconductor component which includes the insulated gate electric field effect **transistor**, through the gate insulator on this well layer, gate electrode 6 and 7 is formed,

**contact diffusion** layer 4 of the same electric **conduction type** as the well layer and 5 puts the gate electrode and the formation is done on the well layer surface, the well layer and the diffusion layer the capacity component which in the counter electrode designates the gate insulator as the capacity insulator film is formed the gate electrode in one electrode. In addition, the territory which includes the impurity of the same electric **conduction type** at a higher density than the well layer is formed to the well layer surface under the gate electrode.

L19 ANSWER 5 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:561646 HCAPLUS
DN 131:164230
TI Integrated circuitry and manufacture of same
IN Wu, Zhiqiang; Tran, Luan C.; Kerr, Robert; Batra, Shubneesh; Yang, Rongsheng
PA Micron Technology, Inc., USA
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 5946564 | A | 19990831 | US 1997-912108 | 19970804 |
| | US 6215151 | B1 | 20010410 | US 1999-255667 | 19990223 |
| PRAI | US 1997-912108 | A3 | 19970804 | | |

AB In one implementation, a common masking step is utilized to provide source/drain diffusion regions and halo **ion implantation** or dopant regions relative to the source/drain regions within one **well region** of a substrate; and well **contact diffusion** regions within another **well region** of the substrate. The common masking step preferably defines at least one mask opening over the substrate within which the well **contact diffusion** region is to be formed, and the mask opening is suitably dimensioned to reduce the amt. of halo **ion implantation** dopant which ultimately reaches the substrate there below. According to one aspect, a plurality of mask openings are provided. According to another aspect, a suitably-dimensioned single mask opening is provided. In yet another aspect, a unique **well region** construction is provided with .gtoreq. 1 complementary mask opening(s) which is configured to, in connection with the provision of the halo **ion implantation** dopant, block the amt. of implantation dopant which ultimately reaches the substrate adjacent the well **contact diffusion** regions. Accordingly, at least some of the well **contact diffusion** region(s) remain in substantial contact with the **well region** after the **doping** of the substrate with the halo **ion implantation** dopant.

RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L19 ANSWER 6 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:276189 HCAPLUS
DN 126:286545
TI Semiconductor devices having double-diffused MOSFETs and fabrication thereof for decreased ON resistance and parasitic function
IN Fujii, Taizo; Hirai, Takehiro; Fujinaga, Kyoo
PA Matsushita Electric Ind Co Ltd, Japan

SO Jpn. Kokai Tokkyo Koho, 19 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 09064218 | A2 | 19970307 | JP 1995-217227 | 19950825 |
| | EP 789401 | A2 | 19970813 | EP 1996-113555 | 19960823 |
| | EP 789401 | A3 | 19980916 | | |
| | R: DE, FR, GB, NL | | | | |
| | US 5817551 | A | 19981006 | US 1996-701913 | 19960823 |
| | US 5905284 | A | 19990518 | US 1997-859366 | 19970520 |
| PRAI | JP 1995-217227 | | 19950825 | | |
| | JP 1995-231189 | | 19950908 | | |
| | US 1996-701913 | | 19960823 | | |

AB The title fabrication involves (1) forming buried drain diffusion layer and 1st body diffusion layer on a semiconductor substrate, (2) forming an **epitaxial layer**, (3) heat-treating to diffuse upwardly the buried drain and body diffusion layers, (4) forming an insulative gate, (5) providing a 2nd body diffusion layer which overlaps a portion of the buried and 1st body diffusion layers over the insulative gate as a mask, and (6) subsequently forming a source diffusion and drain-**contact diffusion** layers over the insulative gate as a mask. The process provides the body dopant concn. with lower concn. on the surface area and higher in the middle layer in the semiconductor substrate. The concn. distribution gives the MOSFETs decreased ON resistance and parasitic characteristics.

L19 ANSWER 7 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:689929 HCAPLUS
DN 125:345890
TI **Integrated circuit** having a vertical Hall element for sensing magnetic fields
IN Biard, James R.
PA Honeywell Inc., USA
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 5572058 | A | 19961105 | US 1995-503167 | 19950717 |

AB A vertical Hall element is formed within an **epitaxial layer** of a semiconductor and isolated from other components by a P-type isolation diffusion. A position-defining diffusion is used to accurately locate a plurality of openings within the position-defining diffusion where **contact diffusions** are made. The position-defining diffusion is done simultaneously with the base diffusion for the **transistors** in the **integrated circuit**, and the **contact diffusions** are done simultaneously with the emitter diffusion for the **transistors** in the **integrated circuit**. Five **contact diffusions** are provided on the upper surface of the **epitaxial layer** and generally aligned within the region defined as the Hall element by the isolation diffusions. The center contact is used to provide elec. current flowing through the Hall element. The elec. current is split and flows to the 2 end **contact**

**diffusions**. The remaining 2 **contact diffusions** are used as sensing contacts and are each placed between the center contact and 1 of the 2 end contacts. By using the openings within the base diffusion, the **contact diffusions** can be accurately located and sized to improve the efficiency, sensitivity, and accuracy of the vertical Hall element. When a magnetic field is imposed perpendicular to the sensing plane of the Hall element and perpendicular to the direction of current flow, the voltage differential between the 2nd and 4th **contact diffusions** is representative of the strength of the magnetic field.

L19 ANSWER 8 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:636313 HCAPLUS
DN 123:72434
TI Bipolar **transistor** and its manufacture
IN Inagaki, Taketoshi
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 07078833 | A2 | 19950320 | JP 1993-223767 | 19930909 |

AB In the title **transistor**, elements are sepd. by trenches. A collector contacting diffusion layer is formed on sides of the trench, which has the same **cond. type** as that of collector and buried diffusion layer. In the manuf., the collector contacting diffusion layer is formed by (1) thermally diffusing dopants into inner surface of the trench, (2) **ion-implanting** dopants diagonally toward inner surface of the trench, or (3) filling the trench with doped film and thermally diffusing the dopants from the film into inner surface of the trench. The method reduces the size of the **transistor**.

L19 ANSWER 9 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:386024 HCAPLUS
DN 122:149322
TI Manufacture of semiconductor devices
IN Miwa, Hiroyuki
PA Sony Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 06188250 | A2 | 19940708 | JP 1992-160267 | 19920527 |
| | US 5352617 | A | 19941004 | US 1993-51520 | 19930426 |
| PRAI | JP 1992-134300 | A | 19920427 | | |
| | JP 1992-160267 | A | 19920527 | | |

AB The title process comprises formation of a buried and an **epitaxial layer**, etching of the **epitaxial layer** except a part of regions for the emitter and the base to be formed, formation of a 1st conductor layer and removal thereof except the draw-out region for the base, removal of the 1st conductor layer in the region for the emitter-base simultaneously with removal of the **epitaxial layer** in the region for the draw-out of the collector, optional

formation of a 2nd conductor, and formation of high concn. diffusion regions for the draw-out of the emitter and the collector using the 2nd conductor as a diffusion source. The 1st and the 2nd conductor may be made of a polycryst. Si or refractory metal-polycryst. Si laminate. A step of **ion implantation** for formation of the diffusion can be omitted with formation of a collector contact.

L19 ANSWER 10 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:497749 HCAPLUS
DN 121:97749
TI Manufacture of semiconductor device for bipolar **transistor**
IN Murata, Tadahiko
PA Yamagata Nippon Denki Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 06120233 | A2 | 19940428 | JP 1992-263370 | 19921001 |

AB The device is manufd. by forming an elec. insulating film on a semiconductor substrate, opening a narrow hole for embedding (A) and a wide hole not for embedding (B), embedding A with a polycryst. Si layer, anisotropic etching the Si layer other than sidewalls in the hole, applying a resin film on B, introducing a x-type impurity (x = elec. **conductive type**) into the Si layer, forming an elec. insulating film, removing the insulating film other than on the Si layer, introducing a y-type impurity (x .noteq. y) into A, heating at high temp. to form an emitter diffusion region and a base **contact diffusion** region, removing the insulating film on the Si layer, and forming an emitter electrode and a base electrode. Over-etching of the elec. insulating film was prevented.

L19 ANSWER 11 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:74090 HCAPLUS
DN 116:74090
TI Manufacture of semiconductor device
IN Terajima, Takami
PA Sanken Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 03206623 | A2 | 19910910 | JP 1990-1974 | 19900109 |
| | JP 2573077 | B2 | 19970116 | | |

AB A method for manufg. a semiconductor device (e.g., an insulated-gate FET) involves: (1) forming an insulating film having a 1st opening on a semiconductor substrate which has an exposed 1st-**cond.-type** 1st semiconductor region; (2) forming a diffusion-preventing cond. mask having a contact to the 1st region via the 1st opening and having a 2nd opening in the 1st opening exposing the 1st region; (3) introducing a 2nd-**cond.-type** impurity into the 1st region via the 2nd opening, and diffusing to form a 2nd semiconductor region connected to the contact; and (4) leaving the mask at least at the contact to form an electrode. Optionally, the cond. of the mask may be

enhanced in the 3rd step. The elec. contact is formed easily by diffusion.

L19 ANSWER 12 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:572534 HCAPLUS
DN 115:172534
TI Manufacture of semiconductor devices
IN Honma, Toshihiro
PA Oki Electric Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 03070143 | A2 | 19910326 | JP 1989-205600 | 19890810 |

AB Manufg. of a semiconductor device having a polysilicon **transistor** laminated on another **transistor** having a common gate contact involves (1) forming the gate contact, depositing a conductive dopant-doped insulative film on the contact and anisotropic etching the insulative film to form a side wall to the gate contact, (2) depositing the polysilicon **transistor** gate insulative film over the gate contact, (3) forming a resist pattern over the polysilicon layer on the gate contact and ion-doping the polysilicon layer over the resist pattern with a dopant having a **cond.-type** same as that in the side wall, and (4) heat-treating to diffuse the ion-dopant and dopant in the side wall into the polysilicon layer. The manufg. arrangement provides a stable relative position for the gate contact and the dopant-diffused layer in the **transistor**.

L19 ANSWER 13 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:190176 HCAPLUS
DN 112:190176
TI Bipolar **transistor** having fluorinated silicon material at the junction
IN Takahashi, Mitsutoshi; Sakakibara, Yutaka
PA Nippon Telegraph and Telephone Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 01272156 | A2 | 19891031 | JP 1988-100242 | 19880425 |

AB The **transistor** has a junction of single-crystal Si and fluorinated amorphous, microcryst., or polycryst. Si, or Si contg. O, C, and/or N. Thus, an npn-bipolar **transistor** manufd. from a single-crystal Si substrate contg. an n-type **epitaxial layer**, a p-type base **contact diffusion** layer, a p-type base layer, an oxide layer, and a contacted n-type amorphous Si layer, prepd. by chem. vapor deposition of a gas mixt. comprising $SiF_4$, H, and $AsH_3$ followed by partial removal to form an emitter, showed good thermal stability.

L19 ANSWER 14 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1981:218581 HCAPLUS
DN 94:218581

TI Schottky barrier diode by **ion implantation** and impurity diffusion
IN Piotrowski, Leo R.
PA Harris Corp., USA
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 4260431 | A | 19810407 | US 1979-106128 | 19791221 |

AB The surface impurity concn. in a substrate having resistivity of 3-20 .OMEGA.-cm is increased, and the resistivity is decreased, by **ion implanting** an n-type impurity and diffusing to a deep depth. A p-type impurity is then diffused into the **ion-implanted** region to form a p-type guard ring, and an n-type impurity is diffused to form a high-concn. (n+) contact region in the **ion-implanted** region outside the guard ring. Metal contacts are then applied and delineated to form a Schottky-barrier contact to the **ion-implanted** region inside the guard ring and an ohmic contact to the n+ contact region. The n+ **contact diffusion** may be deeper than the guard ring and, if desired, may contact a buried m+ region. Std. npn, low-breakdown npn, and Schottky clamped npn bipolar **transistors** may also be formed in the same starting material, in dielec. isolated islands, by the addn. of a 2nd n+ diffusion.

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=> D BIB AB 1-18

L22  ANSWER 1 OF 18  HCAPLUS  COPYRIGHT 2002 ACS
AN   2002:69820  HCAPLUS
DN   136:127626
TI   Horizontal power MOSFETs
IN   Watanabe, Kiminori; Furukawa, Hirokazu; Fujikawa, Toma; Kita, Yasushi;
     Nishijima, Toshifumi
PA   Toshiba Corp., Japan; Toyota Motor Corp.
SO   Jpn. Kokai Tokkyo Koho, 8 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1
     PATENT NO.       KIND  DATE          APPLICATION NO.  DATE
     ---------------  ----  --------      ---------------  --------
PI   JP 2002026315     A2   20020125      JP 2000-205079   20000706
AB   Deep high-d. n-type diffusion layers extending from substrate surface to
     buried layers are formed in the drain regions of the MOSFETs which are
     surrounded by the buried layers, isolation diffusion layers and n-type
     drain contact diffusion regions.  The MOSFETs have
     increased breakdown voltage.

L22  ANSWER 2 OF 18  HCAPLUS  COPYRIGHT 2002 ACS
AN   2001:157018  HCAPLUS
TI   LDMOS type semiconductor device and the production method. [Machine
     Translation].
IN   Negoro,   Takaki
PA   Ricoh Co., Ltd., Japan
SO   Jpn. Kokai Tokkyo Koho, 6 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1
     PATENT NO.       KIND  DATE          APPLICATION NO.  DATE
     ---------------  ----  --------      ---------------  --------
PI   JP 2001060686     A2   20010306      JP 1999-233843   19990820
AB   [Machine Translation of Descriptors].  The LDMOS transistor is
     made small-sized.  The N well diffusion layer 24 which becomes the drain
     in baseplate 22 is done the formation, through the gate oxide membrane 28
     of uniform film thickness to that surface, gate electrode 30 is formed.
     The P type diffusion layer 32 which becomes the channel territory the
     formation is done in the baseplate of source side of gate electrode 30,
     source diffusion layer 34 is formed to the baseplate inside P type
     diffusion layer 32.  Drain contact diffusion layer 36
     is formed inside N well diffusion layer 24 to the baseplate of the site
     which leaves from the drain side end of gate electrode 30.  On the
     baseplate surface under gate electrode 30, source diffusion layer
     diffusion layer territory 32 exists with 34 and well 26 for the drain,
     that territory becomes the channel territory.

L22  ANSWER 3 OF 18  HCAPLUS  COPYRIGHT 2002 ACS
AN   2000:533245  HCAPLUS
TI   Production method of semiconductor device. [Machine Translation].
IN   Tsubaki,   Shigeki
PA   Nec Corp., Japan
SO   Jpn. Kokai Tokkyo Koho, 5 pp.
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CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 2000216261 | A2 | 20000804 | JP 1999-18166 | 19990127 |
| | JP 3225944 | B2 | 20011105 | | |

AB [Machine Translation of Descriptors]. Photolithography the site gap is lost, length of the drain diffusion layer or the source diffusion layer of the FET of contiguity mutually uniformly production method of the semiconductor device which the formation can do is offered. The gate electrode section 3 A which was formed on semiconductor substrate 1, source diffusion layer 7, the **transistor** 20 which with drain diffusion layer 6 is formed continuing, plural as the disposition it is done, the source diffusion layer 7 in each **transistor** 20 which adjoins mutually or drain diffusion layer 6 opposing mutually, in order to be arranged, the gate electrode section 3 A which forms the **transistor** 20 which adjoins mutually the semiconductor device 30 which is formed the formation is done at the time of, adjoining 3 a', after forming, focusing each gate electrode section 3 A and the center section P between 3 a' each gate electrode section 3 A, direction of 3 a' Production method of the semiconductor device where width x1 of the equidistance, the formation does the **contact diffusion** layer 5 which, has the x2 with the next is and, **contact diffusion** layer 5 and particular each gate electrode section 3 A, with 3 a' the formation does drain diffusion layer 6 or source diffusion layer 7.

L22 ANSWER 4 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:227221 HCAPLUS
DN 132:259237
TI Fabrication of a semiconductor device
IN Inaba, Shogo
PA Seiko Epson Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 2000100964 | A2 | 20000407 | JP 1998-265408 | 19980918 |

AB The invention relates to a semiconductor device, i.e., a LDD-structure MOS **transistor**, wherein the occurrence of hot carriers is minimized by varying the offset length and gate oxide thickness of each **transistor**.

L22 ANSWER 5 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:610968 HCAPLUS
DN 131:236761
TI Semiconductor device and fabrication thereof
IN Taki, Masushi
PA Nippon Foundry K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 11261057 | A2 | 19990924 | JP 1998-82719 | 19980313 |

AB The invention relates to a semiconductor device, i.e., a MOS **transistor**, wherein the presence of a channel stopper layer for the buried gate contact allows an optimal threshold voltage without other complications.

L22 ANSWER 6 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:350575 HCAPLUS
DN 130:360123
TI Semiconductor device and manufacture thereof
IN Noda, Kenji
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 11150268 | A2 | 19990602 | JP 1998-218034 | 19980731 |
| | JP 3239940 | B2 | 20011217 | | |
| | TW 408469 | B | 20001011 | TW 1998-87114513 | 19980901 |
| | CN 1211082 | A | 19990317 | CN 1998-117676 | 19980907 |
| PRAI | JP 1997-245387 | A | 19970910 | | |
| | JP 1998-218034 | A | 19980731 | | |

AB The invention relates to a semiconductor device, esp., a MOSFET, wherein the gate contact and the diffusion layer are elec. interconnected automatically by partial removal of the gate sidewall and the spacer during the self-aligned silicide process.

L22 ANSWER 7 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:261964 HCAPLUS
DN 130:290210
TI Fabrication of a semiconductor device
IN Inoue, Akira
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 11111642 | A2 | 19990423 | JP 1997-274710 | 19971007 |
| | JP 3209164 | B2 | 20010917 | | |
| | US 6136699 | A | 20001024 | US 1998-164494 | 19981001 |
| | CN 1213846 | A | 19990414 | CN 1998-121323 | 19981007 |
| PRAI | JP 1997-274710 | A | 19971007 | | |

AB The invention relates to a process for making a semiconductor device, i.e., a MOS **transistor**, suited for use in memory LSI **chips** for computers and communication equipment, wherein the surface of gate contact and source-drain diffusion region is converted to silicides.

L22 ANSWER 8 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:684737 HCAPLUS
DN 129:338767

TI Semiconductor **integrated circuit** and fabrication thereof
IN Asamura, Takeshi
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 10284438 | A2 | 19981023 | JP 1997-83461 | 19970402 |
| | US 2001019162 | A1 | 20010906 | US 2001-813807 | 20010322 |
| PRAI | JP 1997-83461 | A | 19970402 | | |
| | US 1998-52065 | A3 | 19980331 | | |

AB The invention relates to an **integrated circuit**, i.e., a stacked MOS **transistor** LSI, wherein the layout minimizes leak currents in the diffusion layer region interposed between adjacent pair of gate contacts.

L22 ANSWER 9 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:428024 HCAPLUS
DN 129:143744
TI Field effect **transistor**
IN Yamamoto, Teiji; Marukawa, Akira
PA Murata Mfg. Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 10177967 | A2 | 19980630 | JP 1996-353574 | 19961216 |

AB The invention relates to a field effect **transistor**, i.e., a GaAs MESFET, wherein the interdiffusion between the Pt layer and the Au layer in the buried Pt contact is prevented by Mo and/or Ti diffusion barrier layer.

L22 ANSWER 10 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:341460 HCAPLUS
DN 129:75083
TI Manufacture of semiconductor device with lateral bipolar **transistors**
IN Amo, Hiroaki; Kato, Katsuyuki; Miwa, Hiroyuki; Kanematsu, Shigeru
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 10144700 | A2 | 19980529 | JP 1996-293594 | 19961106 |

AB Insulator films (e.g., SiN), which are able to diffuse H2, are formed on semiconductor substrates where **transistor** base regions are formed, contact holes reaching the base regions are formed in the insulator films, emitter and collector regions are formed on the base regions, H2 is supplied to the interface of the substrates and insulator

films by heating in H2, and interconnections from hydrophyllic materials are formed covering the exposed part of the base regions across insulator films. Dangling bonds are unlikely to form at the interface of the substrates and insulator films.

L22 ANSWER 11 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:300755 HCAPLUS
DN 129:48407
TI Standard cells
IN Gion, Masahiro
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 10125787 | A2 | 19980515 | JP 1996-273164 | 19961016 |

AB The area of substrate contact regions is reduced to yield highly **integrated circuits**. **Transistor** source regions and substrate **contact diffusion** regions are located side-by-side and connected across metal silicides, and contact holes for connection with overlying interconnections are formed only on the source regions.

L22 ANSWER 12 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:31281 HCAPLUS
DN 128:109502
TI Body contact structure in semiconductor devices
IN Oh, Kiyon Quon
PA L. G. Semicon Co., Ltd., S. Korea
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 10004192 | A2 | 19980106 | JP 1997-46188 | 19970228 |
| | JP 3008182 | B2 | 20000214 | | |
| | CN 1068458 | B | 20010711 | CN 1997-100726 | 19970226 |
| | CN 1160935 | A | 19971001 | | |
| PRAI | KR 1996-5010 | A | 19960228 | | |

AB The title contact structure comprises a pl. no. of p+-body-**contact diffusion** layers set apart in a row along a channel region on the surface of a p-substrate, n+-source regions each adjacent across along the **contact diffusion** layer, and a pl. no. of contact/circuit metal layers provided to the edge portions on the body-**contact diffusion** layer. The arrangement decreases the differential voltage between the p-substrate and the source in prevention of activation from parasitic components.

L22 ANSWER 13 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:605121 HCAPLUS
DN 129:238710
TI Semiconductor device and its production
IN Cantarini, William F.; Lizotte, Steven C.
PA International Rectifier Corp., USA

SO Ger. Offen., 14 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | DE 19808514 | A1 | 19980910 | DE 1998-19808514 | 19980227 |
| | GB 2322736 | A1 | 19980902 | GB 1998-4274 | 19980227 |
| | FR 2761810 | A1 | 19981009 | FR 1998-2427 | 19980227 |
| | JP 10284591 | A2 | 19981023 | JP 1998-47878 | 19980227 |
| | TW 421850 | B | 20010211 | TW 1998-87102838 | 19980227 |
| | US 2001013627 | A1 | 20010816 | US 2000-746321 | 20001221 |
| PRAI | US 1997-39487P | P | 19970228 | | |
| | US 1998-32495 | B3 | 19980227 | | |

AB N+- or p+-type diffusion regions are formed in a lightly doped p- or n-type semiconductor **wafer**. Spaced individual cells or wells are then formed by an arrangement of intersecting trenches between the p+- (or n+-) diffusion regions. The trenches extend through the device film to a predetd. depth and are filled with a dielec. and polysilicon to isolate the wells from each other. At least 1 diffusion region of each cell is connected to a diffusion region of a neighboring cell to interconnect a predetd. no. of cells. The n+- or p+-diffusion regions can be surrounded by an annular p+- or n+-**contact diffusion** region. A device with MOS gate control (a lateral or vertical MOSFET or IGBT) can be integrated in the same **wafer**.

L22 ANSWER 14 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:656375 HCAPLUS
DN 125:290613
TI Field effect semiconductor devices and manufacture thereof
IN Kuroda, Hideaki
PA Sony Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 08213610 | A2 | 19960820 | JP 1995-42412 | 19950207 |
| | US 5986312 | A | 19991116 | US 1997-922876 | 19970903 |
| PRAI | JP 1995-42412 | | 19950207 | | |
| | US 1996-597872 | | 19960207 | | |

AB The device has a diffusion layer surrounded by an insulating film and device isolation regions, and a conductive film having at least a silicide surface layer, being in contact with the entire surface of the diffusion layer, and covering the insulating film and the device isolation regions. The diffusion layer has a low sheet resistance and is made shallow.

L22 ANSWER 15 OF 18 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:639438 HCAPLUS
DN 119:239438
TI MOS field-effect **transistors** containing ohmic-**contact diffusion** layers
IN Ishii, Masaki
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF

DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 05067633 | A2 | 19930319 | JP 1991-254220 | 19910906 |

AB A diffusion layer, which is formed in the substrate of an MOSFET, and which is not connected with an electrode through a contact hole, has a local ohmic-**contact diffusion** layer inside of it.

L22 ANSWER 16 OF 18 INSPEC COPYRIGHT 2002 IEE DUPLICATE 1
AN 1987:2880506 INSPEC DN B87032704; C87030765
TI The dependence of latch-up sensitivity on layout features in CMOS **integrated circuits**.
AU Song, Y.; Cable, J.S.; Vu, K.N.; Witteles, A.A. (TRW Inc., Redondo Beach, CA, USA)
SO IEEE Transactions on Nuclear Science (Dec. 1986) vol.NS-33, no.6, pt.1, p.1493-8. 9 refs.
Price: CCCC 0018-9499/86/1200-1493$01.00
CODEN: IETNAE ISSN: 0018-9499
Conference: 1986 Annual Conference Nuclear and Space Radiation Effects. Providence, RI, USA, 21-23 July 1986
Sponsor(s): IEEE; DOD; NASA; DOE
DT Conference Article; Journal
TC Practical; Experimental
CY United States
LA English
AB The separated source-to-substrate/well **contact diffusion** layout commonly used in CMOS design has been identified as a primary cause for latch-up sensitivity in bulk CMOS devices. Flash X-ray testing as well as electrical characterization of latch-up has been conducted on test structures which separately contain either separated or butted source-to-substrate/well layout. SPICE simulations using device parameters derived from the PISCES code have been performed to confirm the experimental results. Reduced substrate resistances and field-degraded vertical **transistor** gains are seen to be the reasons for high latch-up immunity of the butted layout. Latch-up-free bulk CMOS **ICs** can be fabricated using the butted-layout design rules, which can eliminate costly hardness assurance measures such as 100% screening.

L22 ANSWER 17 OF 18 INSPEC COPYRIGHT 2002 IEE
AN 1973:571585 INSPEC DN B73038315
TI Manufacturing beam lead, insulated-gate, field effect **transistor** (IGFET) **integrated circuits**.
AU Burock, R.; DeBolt, J.R.; Parente, R.N. (Western Electric Co. Inc., Allentown, PA, USA)
SO Western Electric Engineer (July 1973) vol.17, no.3, p.2-16. 11 refs.
CODEN: WELEAX ISSN: 0043-3659
DT Journal
TC Practical
CY United States
LA English
AB The circuits, which are compatible with bipolar **integrated circuits**, can be operated from a standard 5-volt power supply, because the incorporated devices exhibit a low threshold voltage of -1 volt. The manufacturing process, which in part resembles that used to make bipolar **integrated circuits**, includes the deposition and qualification of doped epitaxial silicon, channel stop

diffusion, source and drain diffusion, substrate **contact diffusion**, gate dielectric formation, contact area window opening, circuit metalization, **wafer** qualification by capacitance-voltage analysis, circuit separation, and automatic testing.

L22 ANSWER 18 OF 18 INSPEC COPYRIGHT 2002 IEE
AN 1970:128776 INSPEC DN B70016633; C70008294
TI Design and fabrication of ECL-**IC**.
AU Hayashi, Y.; Sekigawa, T.; Tarui, Y.
SO Bulletin of the Electrotechnical Laboratory (1969) vol.33, no.6, p.603-10
CODEN: DESIA7 ISSN: 0366-9092
DT Journal
CY Japan
LA Japanese
AB Some problems in the design of high speed ECL and their solutions are described. It is shown that there is a delay which is proportional to the square root of the rise time of input wave form and which must be added to the step response. The base resistance and the collector series resistance have a significant effect on its speed and must be as low as possible. The external base resistance is lowered by p+ base diffusion, while the collector resistance by using a thin epitaxial collector layer, making a buried layer (Ps=22 Omega / Square Operator ) and n+ collector **contact diffusion** surrounding the base region and extending to the buried layer. Additional p+ base diffusion can make the size of **transistors** very small, which results in high speed operation. Finally ECL gates are designed and fabricated using these techniques. The resulting ECL gates have the average propagating delay time of 1.6 ns and the speed power product of 75 pJ. Analysis shows that subnanosecond gates are obtainable using the same **transistor** geometry and technology.

L27 ANSWER 1 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:466363 HCAPLUS
TI Method of fabricating a self-aligned bipolar junction **transistor** in silicon carbide, and resulting devices
IN Singh, Ranbir; Agarwal, Anant K.; Rya, Sei-Hyung
PA Cree, Inc., USA
SO PCT Int. Appl., 30 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | WO 2002049115 | A1 | 20020620 | WO 2000-US33627 | 20001211 |

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

AB A method of fabricating a self-aligned bipolar junction **transistor** in a semiconductor structure having a 1st layer of Si carbide generally having a 1st **cond**. **type** and a 2nd layer of Si carbide generally having a 2nd **cond**. **type**, opposite to the 1st **cond**. **type** is claimed which enables precise and close spacing to the base and emitter contacts. The method comprises forming a pillar in the 2nd Si carbide layer, the pillar having a side wall and defining an adjacent horizontal surface on the 2nd layer, forming an oxide layer having a predetd. thickness on the 2nd semiconductor layer, including the side wall and the horizontal surface. After formation of the oxide layer, the oxide layer on a portion of the horizontal surface adjacent the side wall is anisotropically etched while at least a portion of the oxide layer remains on the side wall, thereby exposing a portion of the horizontal surface. A portion of the 2nd layer below the exposed portion of the horizontal surface is then doped with a dopant of the 1st **cond**. **type** to create a **doped well region** in the 2nd layer which is spaced from the side wall by a distance defined by the thickness of the oxide layer. Resulting devices are likewise disclosed.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 2 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:392103 HCAPLUS
DN 136:394366
TI ESD protection circuit triggered by low voltage
IN Yu, Ta-Lee; Lin, Shi-Tron
PA Winbond Electronics Corp., Taiwan
SO U.S. Pat. Appl. Publ., 9 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|

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PI   US 2002060345     A1   20020523       US 2001-992416   20011116
PRAI TW 2000-89124513  A    20001120
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AB The invention relates to a low-voltage-triggered electrostatic discharge (LVTESD) protection circuit coupled to a pad of an **integrated circuit** (**IC**) to protect core circuits of the **IC** from ESD. The ESD protection circuit comprises a semiconductor substrate having the first **cond. type**, a **well region** having the second **cond. type** is formed in the semiconductor substrate, and an anode-**doped region** having the first **cond. type** and formed in the **well region** to become an anode of a semiconductor control rectifier (SCR). A gate structure is formed in the semiconductor substrate outside the **well region**. A first **doped region** having the second **cond. type** is formed between the **well region** and the gate structure in the semiconductor substrate. A second **doped region** having the second **cond. type** is formed adjacent to the second side of the gate structure in the semiconductor substrate. A plurality of isolated islands are evenly formed and distributed in the first **doped region** so that current in the first **doped region** must flow around the isolated islands to increase the resistance of the first **doped region**.

L27 ANSWER 3 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:353772 HCAPLUS
DN 136:378321
TI MOS-gated power device having segmented trench and extended **doping zone** and process for forming same
IN Kocon, Christopher B.; Grebs, Thomas E.; Cumbo, Joseph L.; Ridley, Rodney S.
PA Fairchild Semiconductor Corporation, USA
SO PCT Int. Appl., 17 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

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     PATENT NO.        KIND  DATE           APPLICATION NO.  DATE
     ---------------   ----  --------       ---------------  --------
PI   WO 2002037569     A2    20020510       WO 2001-US31840  20011011
         W:  DE, JP
         RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL,
             PT, SE, TR
PRAI US 2000-689939    A     20001012
```

AB The invention relates to a trench MOS-gated device comprising a doped monocryst. semiconductor substrate that includes an upper layer and is of a first **conduction type**. An extended trench in the substrate in the upper layer comprises two segments having differing widths relative to one another: a bottom segment of lesser width filled with a dielec. material, and an upper segment of greater width lined with a dielec. material and substantially filled with a conductive material, the filled upper segment of the trench forming a gate region. An extended **doped zone** of a second opposite **conduction type** extends from an upper surface into the upper layer of the substrate only on one side of the trench, and a **doped well region** of the second **conduction type** overlying a drain zone of the first **conduction type** is disposed in the upper layer on the opposite side of the trench. The drain zone is substantially insulated from the extended zone

by the dielec.-filled bottom segment of the trench. A heavily **doped** source **region** of the first **conduction type** and a heavily **doped** body **region** of the second **conduction type** is disposed at the upper surface of the **well region** only on the side of said trench opposite **doped** extended **zone**. An interlevel dielec. layer is disposed on the upper surface overlying the gate and source regions, and a metal layer disposed on the upper surface of the upper layer and the interlevel dielec. layer is in elec. contact with the source and body regions and the extended zone. A process for constructing a trench MOS-gated device comprises: forming in a semiconductor substrate an extended trench that comprises an upper segment and a bottom segment, wherein the bottom segment has a lesser width relative to a greater width of the trench upper segment and extends to a depth corresponding to the total depth of the extended trench. The bottom segment of the trench is substantially filled with dielec. material. The trench upper segment has a floor and sidewalls comprising dielec. material and is substantially filled with a conductive material to form a gate region. A heavily **doped** source **region** of the first **conduction type** and a heavily **doped** body **region** of the second **conduction type** are formed in a surface **well region** on the side of the extended trench opposite an extended **doped zone**.

L27 ANSWER 4 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:251969 HCAPLUS
DN 136:271790
TI MOS-gated power device with doped polysilicon body and process for forming MOS-gated power device
IN Kocon, Christopher B.; Ridley, Rodney S.; Grebs, Thomas E.
PA Fairchild Semiconductor Corporation, USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 6365942 | B1 | 20020402 | US 2000-731169 | 20001206 |

AB An improved MOS-gated power device with a substrate having an upper layer of doped monocryst. Si of a 1st **conduction type** that includes a **doped well region** of a 2nd **conduction type**. The substrate further includes .gtoreq.1 heavily **doped** source **region** of the 1st **conduction type** disposed in a **well region** at an upper surface of the upper layer, a gate region having a conductive material elec. insulated from the source region by a dielec. material, a patterned interlevel dielec. layer on the upper surface overlying the gate and source regions, and a heavily **doped** drain **region** of the 1st **conduction type**. The improvement includes body **regions** contg. heavily **doped** polysilicon of the 2nd **conduction type** disposed in a **well region** at the upper surface of the monocryst. substrate.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 5 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:84068 HCAPLUS

DN 136:143656
TI MOS power semiconductor device having a trench gate and method of making the same
IN Zeng, Jun; Dolny, Gary M.; Kocon, Christopher B.; Brush, Linda S.
PA Fairchild Semiconductor Corporation, USA
SO Eur. Pat. Appl., 7 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | EP 1176643 | A2 | 20020130 | EP 2001-116709 | 20010717 |
| | R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO | | | | |
| | JP 2002124674 | A2 | 20020426 | JP 2001-221780 | 20010723 |
| PRAI | US 2000-624533 | A | 20000724 | | |

AB An MOS power device a substrate comprises an upper layer having an upper surface and an underlying drain region, a **well region** of a 1st **conductance type** disposed in the upper layer over the drain region, and a plurality of spaced apart buried gates, each of which comprises a trench that extends from the upper surface of the upper layer through the **well region** into the drain region. Each trench comprises an insulating material lining its surface, a conductive material filling its lower portion to a selected level substantially below the upper surface of the upper layer, and an insulating material substantially filling the remainder of the trench. A plurality of highly **doped** source **regions** of a 2nd **conductance type** are disposed in the upper layer adjacent the upper portion of each trench, each source region extending from the upper surface to a depth in the upper layer selected to provide overlap between the source regions and the conductive material in the trenches. A groove in each of the highly **doped** source **regions** extends through the source regions into the **well region** and terminates in a nadir. A highly **doped** body **region** of a 1st **conductance type** is disposed in the **well region** adjacent both to the nadir of one or more of the grooves and to adjacent source regions penetrated by the grooves. A conductive layer is disposed over the substrate and elec. contacts the body and source regions. A process for fabricating a device produces an MOS power device that avoids the loss of channel width and provides reduced channel resistance without sacrificing device ruggedness and dynamic characteristics.

L27 ANSWER 6 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:748166 HCAPLUS
DN 135:281712
TI CMOS-compatible lateral DMOS **transistor** and method for producing such a **transistor**
IN Ehwald, Karl-ernst; Heinemann, Bernd; Knoll, Dieter; Winkler, Wolfgang
PA Ihp Gmbh-Innovations for High Performance Microelectronics, Germany
SO PCT Int. Appl., 22 pp.
CODEN: PIXXD2
DT Patent
LA German
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | WO 2001075979 | A1 | 20011011 | WO 2001-DE1175 | 20010324 |

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         W:  JP, US
         RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL,
             PT, SE, TR
     DE 10004387        A1    20011129        DE 2000-10004387 20000331
PRAI DE 2000-10004387  A     20000331
     DE 2000-10063135  A     20001218
```

AB The invention relates to a CMOS-compatible lateral DMOS **transistor** and to a method for producing such a **transistor**. The aim of the invention is to provide a CMOS-compatible DMOS **transistor** that can be optionally designed for very high drain voltages or for the power amplification at very high frequencies by choosing the appropriate layout and that can be produced with little addnl. tech. effort as compared to the conventional sub-.mu.m prodn. technol. for CMOS circuits. To this end, a gate insulator of the inventive CMOS-compatible lateral DMOS **transistor** has a uniform thickness across the entire current-carrying (active) zone below a control gate. Below the control gate, a surface-near zone with increased dopant concn. (**well region**) that dets. the **transistor** threshold voltage is disposed in such a manner that it occupies the entire area below the control gate disposed in the active zone and that it terminates within a so-called drift region between the control gate and a highly-**doped** drain **region**. The entire surface of the drift region is covered by a zone having the **cond**. **type** of the drain region (VLDD) and being poorly doped as compared to the highly **doped** drain **region**.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 7 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:582251 HCAPLUS
DN 135:145731
TI Design and fabrication of self-aligned bipolar junction silicon carbide **transistors**
IN Singh, Ranbir; Agarwal, Anant K.; Ryu, Sei-Hyung
PA USA
SO U.S. Pat. Appl. Publ., 16 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 2001011729 | A1 | 20010809 | US 2001-788689 | 20010219 |
| | US 6329675 | B2 | 20011211 | | |

AB A method is presented for fabricating a self-aligned bipolar junction **transistor** in a semiconductor structure having a 1st layer of SiC generally having a 1st **cond**. **type** and a 2nd layer of SiC generally having a 2nd **cond**. **type**, opposite to the 1st **cond**. **type**. The method comprises forming a pillar in the 2nd SiC layer, the pillar having a side wall and defining an adjacent horizontal surface on the 2nd layer, forming a dielec. layer having a predetd. thickness on the 2nd semiconductor layer, including the side wall and the horizontal surface. After formation of the dielec. layer, the dielec. layer on a portion of the horizontal surface adjacent the side wall is anisotropically etched while at least a portion of the dielec. layer remains on the side wall, thereby exposing a portion of the horizontal surface. A portion of the 2nd layer below the exposed portion of the horizontal surface is then doped with a dopant of the 1st **cond**. **type** to create a **doped well**

**region** in the 2nd layer which is spaced from the side wall by a distance defined by the thickness of the dielec. layer. Resulting devices are likewise disclosed.

L27 ANSWER 8 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:754548 HCAPLUS
DN 133:304554
TI Low voltage dual-well MOS device having high ruggedness, low on-resistance, and improved body diode reverse recovery
IN Zeng, Jun; Wheatley, Carl Franklin, Jr.
PA Intersil Corporation, USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 6137139 | A | 20001024 | US 1999-324553 | 19990603 |
| | EP 1058317 | A2 | 20001206 | EP 2000-401471 | 20000525 |
| | R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO | | | | |
| | JP 2001015755 | A2 | 20010119 | JP 2000-164444 | 20000601 |
| PRAI | US 1999-324553 | A | 19990603 | | |

AB An improved low-voltage MOS device having high ruggedness, low on-resistance, and improved body diode reverse recovery characteristics comprises a semiconductor substrate on which is disposed a doped upper layer of a 1st **conduction type**. The upper layer includes at its upper surface a blanket implant of the 1st **conduction type**, a heavily **doped** source **region** of the 1st **conduction type**, and a heavily **doped** body **region** of a 2nd and opposite **conduction type**. The upper layer further includes a **doped** 1st **well region** of the 1st **conduction type** and a **doped well region** of the 2nd **conduction type** underlying the source and body regions. The 1st **well region** underlies the 2nd **well region** and merges with the blanket implant to form a heavily **doped** neck **region** that abuts the 2nd **well region** at the upper surface of the upper layer. A gate comprising a conductive material sepd. from the upper layer by an insulating layer is disposed on the upper layer overlying the heavily **doped** neck **region**. A process for forming an improved low-voltage MOS device having high ruggedness, low on-resistance, and improved body diode reverse recovery characteristics comprises providing a semiconductor substrate that includes a doped upper layer of a 1st **conduction type**, and implanting a blanket dopant of the 1st **conduction type** in an upper surface of the upper layer. A gate comprising a conductive material and an insulating layer is formed on the upper layer of the substrate, and a **doped** 1st **well region** of the 1st **conduction type** and a **doped** 2nd **well region** of a 2nd and opposite **conduction type** are formed by implanting dopants of 1st and 2nd **conduction types** through a common window into the upper surface of the upper layer. The 1st **well region** underlies the 2nd **well region** and merges with the blanket implant, forming a heavily **doped** neck **region** underlying the gate and abutting the 2nd **well region** at the upper surface of

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     the upper layer.  A heavily doped source region of the
     1st conduction type and a heavily doped body
     region of the 2nd conduction type are formed
     in the 2nd well region at the upper surface of the
     upper layer.
RE.CNT  5      THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
               ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27  ANSWER 9 OF 22  HCAPLUS  COPYRIGHT 2002 ACS
AN   2000:705200  HCAPLUS
DN   133:275203
TI   Power trench MOS-gated device and method of manufacturing it
IN   Kocon, Christopher
PA   Intersil Corp., USA
SO   Eur. Pat. Appl., 14 pp.
     CODEN: EPXXDW
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.        KIND  DATE           APPLICATION NO.  DATE
     ---------------   ----  --------       ---------------  --------
PI   EP 1041640         A2   20001004       EP 2000-104705   20000303
     EP 1041640         A3   20001011
         R:  AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,
             IE, SI, LT, LV, FI, RO
     US 2001001494      A1   20010524       US 1999-283536   19990401
     JP 2000299464      A2   20001024       JP 2000-91296    20000329
PRAI US 1999-283536     A    19990401
AB   A power trench MOS-gated device includes a heavily doped semiconductor
     substrate, a doped upper layer of a 1st conduction type
     on the substrate, and a trench gate in the upper layer that comprises a
     conductive material sepd. from the upper layer by an insulating layer.  An
     enhanced cond. drain region underlies the trench gate, and a heavily
     doped source region of the 1st conduction
     type and a heavily doped body region of a 2nd
     and opposite conduction type are disposed at an upper
     surface of the upper layer.  A deep well region of the
     2nd conduction type underlies the source and body
     regions and extends below the trench gate and abuts the enhanced cond.
     drain region.  A process for forming a power trench MOS-gated device
     comprises providing a semiconductor substrate having a doped upper layer
     of a 1st conduction type.  A dopant of a 2nd and
     opposite conduction type is implanted into an upper
     surface of the upper layer, thereby forming a well
     region in the upper layer, and a layer of nitride is deposited on
     the upper surface.  The nitride layer and upper layer are selectively
     etched to form a trench in the upper layer.  The sidewalls and floor of
     the trench are lined with a thin insulating layer, and a dopant of the 1st
     conduction type is implanted through the thin insulating
     layer on the trench floor, thereby forming an enhanced cond. drain region
     in the upper layer underlying the trench floor.  The thin insulating layer
     is removed from the trench, and a layer of gate insulating material is
     formed on the sidewalls and floors of the trench, which is then
     substantially filled with a conductive material to form a trench gate.
     The nitride layer is removed from the upper surface of the upper layer,
     and the well region in the upper layer is thermally
     diffused, thereby forming a deep well region in the
     upper layer.
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L27 ANSWER 10 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:238091 HCAPLUS
DN 132:259278
TI Semiconductor device including protective circuit with guard ring for MOS **transistor**
IN Higuchi, Tsutomu; Yamada, Hitoshi
PA Oki Electric Industry Co., Ltd., Japan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 6049111 | A | 20000411 | US 1998-12971 | 19980126 |
| | JP 11026695 | A2 | 19990129 | JP 1997-190416 | 19970630 |

PRAI JP 1997-190416 19970630

AB A semiconductor device includes a protection circuit and a guard ring. The guard ring is formed between a MOS **transistor** of a semiconductor substrate and internal circuits, to cut off a leakage current from the MOS **transistor** to the internal circuits. The guard ring includes a **well region** and a pair of heavily **doped** impurity **regions** for med spaced apart from each other on the surface of the **well region**. The pair of **doped regions** have mutually different **cond**. **types** and have substantially equal voltages applied to have potentials with respect to the source of the MOS **transistor**. There are formed a 1st parasitic **transistor** having one heavily **doped** impurity **region** as the collector, the semiconductor substrate as the base, and the drain of the MOS **transistor** as the emitter, the one heavily **doped** impurity **region** being identical in **cond**. **type** with the **well region**; and a 2nd parasitic **transistor** having the other heavily **doped** impurity **region** as the emitter, the **well region** as the base, and the semiconductor substrate as the collector. When the 1st parasitic **transistor** conducts, the 2nd parasitic **transistor** conducts, which turns off the 1st parasitic **transistor**. Thus, the leakage current is prevented from flowing from the MOS **transistor** through the 1st parasitic **transistor** to the internal circuits.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 11 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:166367 HCAPLUS
DN 132:215681
TI Semiconductor device fabrication
IN Masuoka, Hiroaki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 2000077661 | A2 | 20000314 | JP 1998-246071 | 19980831 |

AB A method for fabricating a semiconductor device such as a MOSFET involves

forming element-isolation regions in a substrate, forming **well regions** having a first **cond. type**, forming an insulator film such as SiO2 on the **well regions**, forming a dummy gate pattern, forming counter-**doping regions** by oblique-angle ion implantation from the 2 gate-length directions, forming a gate oxide film, depositing a polysilicon film, planarizing to expose the insulator film to form a gate electrode, removing the insulator film, forming LDD regions by ion implantation, forming an oxide gate side wall, and forming source/drain regions by ion implantation. A uniform threshold voltage is obtained even when the gate lengths vary. .

L27 ANSWER 12 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:28347 HCAPLUS
DN 124:74035
TI Power **integrated circuit** structure with a vertical IGBT, and its manufacture
IN Zambrano, Raffaele
PA Consorzio per la Ricerca sulla Microelettronica nel Mezzogiorno, Italy
SO Eur. Pat. Appl., 14 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| | --------------- | ---- | -------- | --------------- | -------- |
| PI | EP 683529 | A1 | 19951122 | EP 1994-830230 | 19940519 |
| | R: DE, FR, GB, IT | | | | |
| | JP 07321321 | A2 | 19951208 | JP 1995-117168 | 19950516 |
| | US 5703385 | A | 19971230 | US 1995-443908 | 19950517 |
| | US 5556792 | A | 19960917 | US 1995-472196 | 19950607 |
| PRAI | EP 1994-830230 | | 19940519 | | |
| | US 1995-443908 | | 19950517 | | |

AB A power **integrated circuit** structure comprises a lightly doped semiconductor layer of the 1st **cond. type** superimposed over a heavily doped semiconductor substrate of a 2nd **cond. type**, in which a vertical IGBT and driving and control circuitry comprising at least 1st-**cond.**-**type** -channel MOSFETs are integrated; the MOSFETs are obtained inside **well regions** of the 2nd **cond. type** which are included in .gtoreq.1 lightly **doped region** of the 1st **cond. type** completely surrounded by and isolated from the lightly doped layer of the 1st **cond. type** by means of an isolated region of the 2nd **cond. type**.

L27 ANSWER 13 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:661125 HCAPLUS
DN 123:129848
TI Method for improving latchup immunity in a dual-polysilicon gate process
IN Manning, Monte
PA Micron Semiconductor, Inc., USA
SO U.S., 18 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| --------------- | ---- | -------- | --------------- | -------- |

| | | | | | |
|---|---|---|---|---|---|
| PI | US 5420061 | A | 19950530 | US 1993-106179 | 19930813 |
| | US 5801423 | A | 19980901 | US 1996-762741 | 19961210 |
| | US 6207512 | B1 | 20010327 | US 1998-126057 | 19980730 |
| | US 2002003266 | A1 | 20020110 | US 1998-126182 | 19980730 |
| PRAI | US 1993-106179 | A3 | 19930813 | | |
| | US 1995-390605 | B1 | 19950217 | | |
| | US 1996-762741 | A1 | 19961210 | | |

AB The invention is a method for creating a portion of an **integrated circuit** on a semiconductor **wafer**. The invention comprises doping a substrate to form a **doped well region** having the opposite **cond. type** to the substrate. Sep. photomasking steps are used to define N- and P-channel MOS **transistor** gates. A trench is formed near the well without using addnl. masking steps. The trench improves the latchup immunity of the device. Thus, the invention improves latchup immunity without addnl. process complexity.

L27 ANSWER 14 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:511468 HCAPLUS
DN 122:253841
TI Manufacture of complementary MOS semiconductor devices
IN Akasaka, Yasushi; Ono, Tamashiro; Arai, Hideaki; Saito, Masanobu; Yoshitomi, Takashi; Iwai, Hiroshi
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 17 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 06236967 | A2 | 19940823 | JP 1993-102867 | 19930428 |
| | JP 3200231 | B2 | 20010820 | | |
| PRAI | JP 1992-333193 | A | 19921214 | | |

AB The title process comprises formation of an n- and/or p-MOS **well region**, and device isolation **regions**, **doping** of an impurity into the **well regions** for control of threshold values, selective epitaxial growth of Si on the unmasked device region by masking the n-MOS or the p-MOS device region, removal of the mask, deposition of a gate oxide and a polycryst. film, and patterning thereof to form the gate electrode. The process may comprise (1) diffusion of an impurity into channel **region** from a **doped** silicate glass film by heat treatment and/or (2) deposition of a silicate glass film doped with a 1st **cond. type** impurity on the device region, implantation of a 2nd **cond. type** impurity through the silicate glass film forming a 1st impurity layer, and diffusion of the 1st **cond. type** impurity forming a 2nd impurity layer in the 1st impurity layer. A low concn. surface channel MOSFET and buried channel MOSFET are formed on a substrate, and decrease of carrier mobility and short channel effect are suppressed.

L27 ANSWER 15 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:571756 HCAPLUS
DN 119:171756
TI Semiconductor devices and fabrication thereof
IN Mizuno, Tomohisa; Asao, Yoshiaki
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 04346272 | A2 | 19921202 | JP 1991-118963 | 19910524 |
| | JP 3100663 | B2 | 20001016 | | |
| | US 5696401 | A | 19971209 | US 1996-623941 | 19960329 |
| PRAI | JP 1991-118963 | A | 19910524 | | |
| | US 1992-885441 | B1 | 19920520 | | |
| | US 1993-167125 | B1 | 19931216 | | |
| | US 1995-516961 | B1 | 19950818 | | |

AB The title fabrication of a MOS FET involves forming a 1st **cond.-type** 1st **well region** on a 2nd **cond.-type** semiconductor substrate, forming a thin insulator film on the substrate, forming a gate contact on the insulator film, doping the substrate over the gate contact mask with a 2nd **cond.-type** dopant to prep. a diffusion **region**, and **doping** with a 1st **cond.-type** dopant to prep. a 1st **cond.-type** 2nd **well region** which is formed to surround the the diffusion region. The fabrication provides the depth change of the **well region** with its channel region and the diffusion region so as to sustain the charge amt. in its depletion layer.

L27 ANSWER 16 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:203401 HCAPLUS
DN 118:203401
TI Semiconductive MOS **integrated circuits**
IN Suzuki, Koichi; Miyoshi, Norihito; Inoue, Osamu
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 04258173 | A2 | 19920914 | JP 1991-20150 | 19910213 |

AB The title circuit comprises (1) a 1st **transistor** having a 1st **cond.-type** drain region formed on a 2nd **cond.-type** semiconductor substrate, a 2nd **cond.-type well region** and a highly-doped 1st. **cond.-type** source region formed on the drain region, and a common source region provided with the substrate by sepg. the drain region with a 1st **cond.-type** insulating region and (2) a 2nd **transistor** having a highly doped 1st **cond.-type** region buried at the bottom of the 1st **cond.-type** drain **region**, a highly-**doped** 1st **cond.-type** lead region extended from the buried region to the surface of the drain region, and a common drain region provided with the buried region. The arrangement gives multiple **transistors** without an increase of its **chip** surface area.

L27 ANSWER 17 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:418596 HCAPLUS
DN 117:18596
TI Manufacture of vertical MOS FET

IN Yamamoto, Masanori
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 04011740 | A2 | 19920116 | JP 1990-114415 | 19900428 |
| | JP 2987875 | B2 | 19991206 | | |

AB A method for manufg. a vertical MOS FET involves the following steps: (1) forming a 2nd-**cond**.-**type** **well** **region** in a 1st-**cond**.-**type** semiconductor substrate; (2) implanting ions into the bottom of the **well** **region** at a high energy to form a 1st-**cond**.-**type** heavily **doped** **region**; (3) forming a gate insulating film and gate electrode on the substrate; (4) forming a 2nd-**cond**.-**type** base region in the **well** **region**; and (5) forming a 1st-**cond**.-**type** source region in the base region. By having the heavily **doped** **region**, the **well** **region** gives an improved withstand voltage.

L27 ANSWER 18 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:97263 HCAPLUS
DN 116:97263
TI Bipolar **transistors** and semiconductor devices therewith
IN Tanba, Akihiro; Akiyama, Noboru; Kobayashi, Yutaka; Miyazawa, Hideyuki; Murata, Jun; Miyazawa, Kazuyuki
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 03159129 | A2 | 19910709 | JP 1989-297359 | 19891117 |

AB The **transistor** comprises: (A) a base electrode formed on a semiconductor substrate; (B) a high-**doped** emitter **region**; (C) a high-**doped** collector **region**; (D) a base region surrounding (A), wherein (B), (C) are 1st **cond**.-**type** and are self-aligned with (A); and (D) is 2nd **cond**.-**type**. The device comprises a linear coupling of bipolar and MOS field-effect **transistors**, wherein (B)-(C) of the former and the p-**well** **region** of the latter are formed by the same process. The device has a low current threshold for both input and substrate.

L27 ANSWER 19 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:74125 HCAPLUS
DN 116:74125
TI Manufacture of complementary-type semiconductor device
IN Yoshida, Toru; Koyama, Hirosuke; Sakamoto, Takashi
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 03215971 | A2 | 19910920 | JP 1990-11231 | 19900120 |

AB A method for manufg. a complementary-type semiconductor device (MOS **transistor**) involves following steps: (1) forming a 2nd **cond.-type well region** on a 1st **cond.-type** semiconductor substrate; (2) forming a 1st conductor film, and patterning to have a gate electrode pattern using a 1st photosensitive resin film; (3) implanting 2nd **cond.-type** 1st impurity ions into a substrate for a lightly-**doped** drain **region** without removing the 1st resin film; (4) coating a 2nd photosensitive resin film without removing the 1st resin film, and patterning only in the **well region**; and (5) implanting the 2nd **cond.-type** 2nd impurity ions into the wall region using the 2nd resin film as a mask for forming a punch-through stopper.

L27 ANSWER 20 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1986:489618 HCAPLUS
DN 105:89618
TI Semiconductor **integrated circuit**
IN Nojiri, Kazuo; Tsukuni, Kazuyuki
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 61032440 | A2 | 19860215 | JP 1984-152882 | 19840725 |

AB A semiconductor **integrated circuit** is produced by (1) forming a depression on a 1st-**cond.-type** semiconductor substrate; (2) forming an insulating film on the side wall of the depression for isolation; (3) growing an epitaxial layer and implanting a 2nd-**cond.-type** impurity into the epitaxial layer; (4) continuing the epitaxial growth until an even surface is attained; and (5) forming a 2nd **cond. type** semiconductor region by further diffusion of the impurity. The 2nd-**cond.-type** semiconductor region may be used for formation of a complementary MIS, and may have a higher impurity concn. at the bottom than that at the surface. Thus, a depression 5 .mu.m deep was formed on an n-Si substrate, using a SiO2 film as a mask. Isolation layers of SiO2 0.1-0.3 .mu.m thick on the side wall of the depression were formed. An epitaxial Si layer 1.5-2.5 .mu.m thick was grown and B+ was implanted at 1014-1015 cm2 to a depth of 0.15-0.3 .mu.m. The epitaxial Si layer was continuously grown, and a p-**well region** was formed in the epitaxial layer by heat-treatment at 1100.degree.. The product prevented decrease of mobility in the complementary MIS.

L27 ANSWER 21 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1986:60522 HCAPLUS
DN 104:60522
TI Semiconductor **integrated circuits**
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese

FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 60097661 | A2 | 19850531 | JP 1983-204799 | 19831102 |
| | JP 06022274 | B4 | 19940323 | | |

AB **Integrated circuits** having bipolar **transistors** and compensation-type insulator-gate field-effect **transistors** (MIS FET) formed in an epitaxial semiconductor layer of a 2nd **cond**. **type** grown on a semiconductor substrate of a 1st **cond**. **type** are claimed in which insulator isolation regions are formed at the boundary between the bipolar **transistor** and MIS FET region and at the boundary between the **well region** of the 2nd **cond**. **type** for forming the 1st channel type MIS FET and the **well region** of 1st **cond**. **type** for forming the 2nd channel type MIS FET, and the depth of the isolation regions is such that the isolation regions are in contact with the semiconductor substrate. Optionally, **doped** semiconductor **regions** having 2nd **cond**. **type** impurities (concn. greater than that in the epitaxial layer) are formed at the epitaxial layer-substrate interface regions corresponding to the **well regions** of the 1st channel type MIS FET and the bipolar **transistor** regions, whereas a high concn. **doped** **region** contg. 1st **cond**. **type** impurities is formed in the interface regions corresponding to the **well** **regions** of the 2nd channel type MIS FET. The depth of the isolation regions selected for the above **integrated** **circuit** ensures the elec. isolation of the **integrated** **circuit** components.

L27 ANSWER 22 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1985:104603 HCAPLUS
DN 102:104603
TI **Doping** field isolation **regions** in CMOS **integrated circuits**
IN Haskell, Jacob D.
PA Advanced Micro Devices, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 4481705 | A | 19841113 | US 1983-504193 | 19830614 |

AB A process is described for fabricating complementary **transistors** in a semiconductor substrate having a first **cond**. **type** **well region** in an opposite **cond**. **type** substrate beneath regions of oxidized Si. The improvement of the process consists of introducing a field implant by using a process including the steps of fabricating a first mask over the substrate except where field regions are desired, introducing p-type impurity into the unmasked regions, oxidizing the Si substrate except where overlayed by the first mask to form field regions, fabricating a 2nd mask over the semiconductor substrate except for 2nd field regions, introducing n-**cond**. **type** impurity into the 2nd field regions, and oxidizing the substrate to form the 2nd field region. In an example, a complementary MOS (CMOS) device is formed on an n-type Si substrate by using Si nitride as the masking layers, B is the p-type impurity and As as the n-type impurity.

L29 ANSWER 1 OF 31 INSPEC COPYRIGHT 2002 IEE
AN 1971:305716 INSPEC DN B71033359
TI Semiconductor **integrated circuit**.
CS Mullard Ltd
PI UK 1237712 30 June 1971
AD 30 Aug. 1968
PRAI UK 41475/68
DT Patent
TC Practical
CY United Kingdom
LA English
AB It consists of a substrate of semi-conductor material carrying an **epitaxial layer** on one surface with regions in the layer and substrate providing one or more **transistors** etc. A **transistor** has an emitter region of one **conductivity type** lying within a base region of opposite **conductivity type** which in turn lies within the collector region of the one **conductivity type**. The substrate is of opposite **conductivity type** with some of the regions extending through the layer and into the substrate. The regions are formed by doping concentrations having impurity concentrations such as to give the desired characteristics to the, or each **transistor** and associated circuitry.

L29 ANSWER 2 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:290740 HCAPLUS
DN 136:302770
TI Manufacture of lateral FET having source contact to substrate with low resistance
IN Leong, Siew Kok
PA Polyfet RF Devices, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 6372557 | B1 | 20020416 | US 2000-552239 | 20000419 |

AB A method for forming a lateral DMOS **transistor** comprises: (a) forming a first **doped region** of a first **cond. type** in a semiconductor substrate of the first **cond. type**; (b) forming an **epitaxial layer** on the substrate; (c) forming a second **doped region** of the first **cond. type** in the **epitaxial layer**; and (d) forming a body region of the first **cond. type** in the **epitaxial layer**. The process of forming the first and second **doped regions** and the body region includes thermally diffusing dopants in these regions so that the first and second **doped regions** diffuse and meet one another. The body region also meets and contacts the second **doped region**. The body region is elec. coupled to the substrate via the first and second **doped regions**. Source and drain regions are then formed in the **epitaxial layer**. By forming the **transistor** in this manner, the elec. resistance between the body region and substrate can be reduced or minimized. Also, the size of the **transistor** can be reduced,

compared to prior art lateral DMOS **transistors**.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 3 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:762417 HCAPLUS
DN 135:312185
TI Semiconductor device.
IN Furukawa, Akihiko; Sugahara, Kazuyuki
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 2001291863 | A2 | 20011019 | JP 2000-106369 | 20000407 |

AB A semiconductor device comprises an element-isolation region having an insulator film on a semiconductor substrate having a first **cond. type**, a conductor wiring extending over the element-isolation **region**, a first **doped region** having the first **cond. type** on the substrate side on which a substrate potential is applied, and a second **doped region** having the concn. of a first **cond. type** impurity higher than the substrate at the region extending from the bottom of the element-isolation region to the first **doped region**. Specifically, the substrate may comprises a Si substrate having a Si **epitaxial layer**. The device is useful as a high-frequency Si MOSFET having a decreased thermal noise.

L29 ANSWER 4 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:861116 HCAPLUS
DN 134:35899
TI Fabrication of VDMOS structure with reduced parasitic effects
IN Frisina, Ferruccio
PA Stmicroelectronics S.r.L., Italy
SO Eur. Pat. Appl., 12 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | EP 1058303 | A1 | 20001206 | EP 1999-830334 | 19990531 |
| | R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO | | | | |
| | US 6391723 | B1 | 20020521 | US 2000-583458 | 20000531 |
| PRAI | EP 1999-830334 | A | 19990531 | | |

AB A fabrication method consists of forming a properly **doped** diffused body **region**, and then forming a resist mask that defines the implantation apertures of the source region inside the body region previously formed by implantation and diffusion of the dopant. Through this resist mask a dopant of the same **cond. type** of the preformed body region is implanted at a sufficiently high kinetic energy, such that the implantation may extend down to a certain depth from the surface of the semiconductor substrate. Another dopant of **cond. type** opposite to the cond. of the dopant used to realize the body regions is implanted through the same mask. The

implantation of this other dopant is performed at a lower kinetic energy than is used to implant the dopant of the highly **doped** buried body **region**, so as to constitute source regions geometrically above the highly **doped** buried body **region** in a superficial zone of the body region. An effective gain redn. of the parasite **transistor** is achieved without the need of a dedicated masking step.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L29 ANSWER 5 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:481263 HCAPLUS
DN 133:67229
TI Bipolar **transistor** and manufacture thereof
IN Yeum, Byung-ryul; Kang, Sang-won; Lee, Kyung-soo
PA Korea Electronics + Telecommunications Research Institute, S. Korea; Korea Telecom
SO Repub. Korea, No pp. given
CODEN: KRXXFC
DT Patent
LA Korean
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | KR 9606750 | B1 | 19960523 | KR 1992-15842 | 19920901 |

AB The bipolar **transistor** comprises: a semiconductor substrate; a first **epitaxial layer** (1) doped with impurities; a second **epitaxial layer** (2) formed on top of the first **epitaxial layer** (1); a local oxide film (3) sepg. and limiting active and inactive areas ; a first **conductive type** base area (5) formed on top of the second **epitaxial layer** (2); a first **conductive type** base link (11) doped with impurities; a first low resistant layer (6) of the first **conductive type** doped with impurities formed on top of the base area (5); a second **conductive type** emitter **area** (14a) **doped** with impurities formed on top of base area (5); a second **conductive type** collector **area** (9) **doped** with impurities; a second low resistant layer (14b) of the second **conductive type** formed on upper part of the above collector area (4); and a base electrode, collector electrode and an emitter electrode (16).

L29 ANSWER 6 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:384620 HCAPLUS
DN 132:355756
TI Trench-gate semiconductor devices and their manufacture
IN Hurkx, Godefridus A. M.; Hueting, Raymond J. E.
PA Koninklijke Philips Electronics N.V., Neth.
SO PCT Int. Appl., 22 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | WO 2000033386 | A2 | 20000608 | WO 1999-EP8951 | 19991116 |
| | WO 2000033386 | A3 | 20001116 | | |

W: JP
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL,

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          PT, SE
     EP 1066652          A2    20010110        EP 1999-956024   19991116
         R:  AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,
             IE, FI
PRAI GB 1998-26041       A     19981128
     WO 1999-EP8951      W     19991116
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AB In a trench-gate semiconductor device, for example a cellular power MOSFET, the gate (11) is present in a trench (20) that extends through the channel-accommodating region (15) of the device. An underlying body portion (16) that carries a high voltage in an off state of the device is present adjacent to a side wall of a lower part (20b) of the trench (20). Instead of being a single high-resistivity region, this body portion (16) comprises 1st regions (61) of a 1st **cond**. **type** interposed with 2nd regions (62) of the opposite 2nd **cond**. **type**. In the conducting state of the device, the 1st regions (61) provide parallel current paths through the thick body portion (16), from the conduction channel (12) in the channel-accommodating region (15). In an off-state of the device, the body portion (16) carries a depletion layer (50). The 1st region (61) of this body portion (16) is present between the 2nd region (62) and the side wall (22) of the lower part (20b) of the trench (20) and has a doping concn. (Nd) of the 1st **cond**. **type** that is higher than the doping concn. (Na) of the 2nd **cond**. **type** of the 2nd region (62). A balanced space charge is nonetheless obtained by depletion of the 1st and 2nd regions (61, 62), because the width (W1) of the 1st region (61) is made smaller than the width (W2) of the lower-**doped** 2nd **region** (62). This device structure can have a low on-resistance and high breakdown voltage, while also permitting its com. manuf. using dopant out-diffusion from the lower trench part (20b) into the lower-**doped** 2nd **region** (62) to form the 1st region (61).

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L29  ANSWER 7 OF 31  HCAPLUS  COPYRIGHT 2002 ACS
AN   1997:506786  HCAPLUS
DN   127:129720
TI   Resurf semiconductor device and its manufacture
IN   Ludikhuize, Adrianus Willem
PA   Philips Electronics N.V., Neth.; Philips Norden Ab
SO   PCT Int. Appl., 14 pp.
     CODEN: PIXXD2
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.          KIND  DATE            APPLICATION NO.  DATE
     ---------------     ----  --------        ---------------  --------
PI   WO 9723901          A1    19970703        WO 1996-IB1334   19961203
         W:  JP, KR
         RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE
     EP 811242           A1    19971210        EP 1996-938418   19961203
         R:  DE, FR, GB, IT, NL
     US 5976942          A     19991102        US 1996-770030   19961219
PRAI EP 1995-203584            19951221
     WO 1996-IB1334            19961203
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AB An **epitaxial layer** with a doping of .apprx.1012 atoms/cm2 is used in accordance with the resurf condition for the high-voltage circuit element in high-voltage **integrated circuits** of the resurf type. If the circuit comprises a region in the **epitaxial layer** which is of the same **cond** . **type** as the substrate, and to which a high voltage is applied, the **doping** between this **region** and the substrate must

in addn. be sufficiently high to prevent punchthrough between the region and the substrate. A known method of complying with these 2 requirements is to make the **epitaxial layer** very thick. It is found in practice, however, that this method is often not very well reproducible. According to the invention, the **epitaxial layer** is provided in the form of a high-resistivity layer which is doped from the upper side and from a buried layer. The buried layer is blanket-deposited, which dispenses with a masking step, and is locally redoped by the island insulation region.

L29 ANSWER 8 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:689860 HCAPLUS
DN 123:72159
TI Manufacture of semiconductor devices
IN Nakabayashi, Masahiko
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 06318603 | A2 | 19941115 | JP 1993-127980 | 19930504 |
| | JP 2500597 | B2 | 19960529 | | |

AB The title process comprises formation of a 1st insulating film on a 1st **cond. type** semiconductor substrate and etching thereof leaving vertical sides, thermal oxidn. of exposed surface of an **epitaxial layer** forming a 2nd insulating film, formation of an oxidn.-resistant 3rd insulating film on the entire surface and anisotropic etching thereof leaving the film on the side walls of the 1st insulating film, formation of device isolation regions by oxidn., removal of the 3rd insulating film and the 2nd insulating film thereunder, formation of a 1st polycryst. Si film and doping of a 2nd **cond. type** impurity into a part thereof, formation of a 4th insulating film on the entire surface and an even surface film, diffusion of the impurity in the 1st polycryst. Si film into the **epitaxial layer**, exposure of the 1st insulating film without exposing the 1st polycryst. Si film on the device isolation regions, removal of the 1st insulating film exposed forming a depression, formation of a 1st $SiO_2$ film on the epitaxial and the 1st polycryst. Si layer exposed in the depression, formation of the base **region** by **doping** of a 2nd **cond. type** impurity into the **epitaxial layer**, formation of a 5th insulating film on the entire surface and removal thereof except the side walls of the depression by anisotropic etching, and removal of the $SiO_2$ film on the bottom of the depression,. Formation of a 2nd polycryst. Si film doped with a 1st **cond. type** impurity in the depression, and formation of the emitter region by diffusion of the impurity from the 2nd polycryst. Si film into the **epitaxial layer**. The device isolation regions, the base, a draw-out region for the base, and the emitter are formed in self-alignment by a single photolithog. step, and the device area is decreased for integration and collector-base junction capacitance is lowered with decrease of the base area.

L29 ANSWER 9 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:71766 HCAPLUS
DN 118:71766
TI Semiconductor **integrated circuit**

IN Ono, Hajime
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 04177840 | A2 | 19920625 | JP 1990-306552 | 19901113 |
| | JP 3128818 | B2 | 20010129 | | |

AB A semiconductor **integrated circuit** comprises an **epitaxial layer** having a 2nd **cond.** **type** on a semiconductor substrate having a 1st **cond.** **type**, a base layer having the 1st cond. in the **epitaxial** **layer**, an emitter layer having the 2nd **cond.** **type** in the base layer, and an insulat.omega.r layer passing through the emitter and base layers. The **epitaxial** **layer** has a high-impurity-concn. layer having the 2nd **cond** . **type** directly below the insulator layer to prevent dipping out the base.

L29 ANSWER 10 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:583082 HCAPLUS
DN 117:183082
TI Manufacture of bipolar semiconductor devices
IN Takahashi, Sanekatsu
PA Nippon Denki K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 04099330 | A2 | 19920331 | JP 1990-217699 | 19900818 |
| | JP 2943280 | B2 | 19990830 | | |

AB The title manufg. involves (1) forming a 1st **cond.-type** dopant-diffusion collector region and a 1st **epitaxial** **layer** on a semiconductor substrate, (2) forming a highly concd. 1st **cond.-type** 2nd **doped area** in a base region area on the 1st **epitaxial layer**, (3) forming a 2nd **cond.-type** 2nd **epitaxial** **layer** as a base region over the 2nd **doped area** , and (4) forming a highly concd. 1st **cond.-type** emitter region on the 2nd **epitaxial layer**. The manufg. arrangement prevents the base region depth increase which may otherwise caused by annealing.

L29 ANSWER 11 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:583081 HCAPLUS
DN 117:183081
TI Manufacture of semiconductor devices having a bipolar **transistor** with a high cut-off frequency
IN Miyazaki, Shinichi
PA Nippon Denki K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent

LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 04099329 | A2 | 19920331 | JP 1990-217698 | 19900818 |

AB The title manufg. involves (1) forming a 1st **cond.-type** highly doped **epitaxial layer** in an emitter region area on a 1st **cond.-type** collector region of a semiconductor layer, (2) forming a 1st **cond.-type** lightly doped **epitaxial layer** outside the highly **doped area**, (3) forming a 2nd **cond.-type** epitaxial base layer over the highly and lightly **doped areas**, and (4) forming a 1st **cond.-type** emitter region in the 2nd **cond.-type** epitaxial region. The epitaxy for the formation of the highly **doped region** prevents the collector from damages caused by doping.

L29 ANSWER 12 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:74114 HCAPLUS
DN 116:74114
TI Mini MIS field-effect **transistors** and manufacturing thereof
IN Kusunoki, Shigeru; Komori, Shigeki; Tsukamoto, Katsuhiro
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 22 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 03209876 | A2 | 19910912 | JP 1990-5161 | 19900112 |
| | US 5196908 | A | 19930323 | US 1991-637871 | 19910108 |
| | US 5330923 | A | 19940719 | US 1992-980408 | 19921120 |
| | US 5448093 | A | 19950905 | US 1994-233553 | 19940426 |
| PRAI | JP 1990-5161 | | 19900112 | | |
| | US 1991-637871 | | 19910108 | | |
| | US 1992-980407 | | 19921120 | | |

AB The title microtransistor comprises (1) 1st **cond.-type** source and drain regions formed apart by a clearance .ltoreq.2 .mu.m each other on a semiconductor layer, (2) a 2nd **cond.-type** channel layer doped at .ltoreq.1.times.1016/cm3 and formed between the source and drain regions at a depth shallower than the doped depth of the regions, and (3) a 2nd **cond.-type** threshold-voltage-controlling **region doped** at .gtoreq.1.times.1017/cm3 formed below the channel layer. Manufg. of the mini MIS FETs involves formation of a channel layer doped at .gtoreq.1.times.1017/cm3 to a certain depth and prepd. in its length .ltoreq.2 .mu.m between the source and drain regions by process comprising (1) prepg. a 2st **cond.-type** semiconductor layer doped at .gtoreq.1.times.1017/cm3 to a certain depth, (2) crystal growing a 1st **cond.-type** **epitaxial layer** doped at .ltoreq.1.times.1016/cm3 on its surface, and (3) forming a 2nd **cond.-type** source and drain regions provided apart by a clearance .ltoreq.2 .mu.m each other to a depth lower than the bottom of the **epitaxial layer**. The arrangement gives mini, high-carrier-transferring, high-speed MIS FETs.

L29 ANSWER 13 OF 31 HCAPLUS COPYRIGHT 2002 ACS

AN 1991:692943 HCAPLUS
DN 115:292943
TI Manufacture of semiconductor device
IN Gomi, Takayuki; Miwa, Hiroyuki; Kashiwanuma, Akio
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 03214664 | A2 | 19910919 | JP 1990-9622 | 19900119 |

AB A method for manufg. a semiconductor device (e.g., a bipolar **transistor**) to form an element isolation by an insulating film and a 1st-**cond**.-**type** **doped** **region** under the insulating film involves: (1) forming a 2nd-**cond**.-**type** buried region in a prescribed region of a 1st-**cond**.-**type** semiconductor substrate at a low concn.; (2) introducing the 1st **cond**.-**type** impurity on the entire surface of the substrate to raise the concn.; (3) forming a 2nd-**cond**.-**type** **epitaxial** **layer** on the entire surface; and (4) forming the insulating film and the 1st **cond**.-**type** **doped** **region** under the insulating film and reaching the substrate. The diffusion of the impurity in the **epitaxial** **layer** is controlled by the **doped** **region**, and the element-substrate capacitance is decreased.

L29 ANSWER 14 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:596024 HCAPLUS
DN 115:196024
TI Manufacture of vertical field-effect **transistors**
IN Sawada, Masami
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 03034376 | A2 | 19910214 | JP 1989-169450 | 19890629 |

AB The title manuf. involves (1) epitaxy of a 2nd **cond**.-**type** material on a 1st **cond**.-**type** semiconductive substrate to form a gate insulator film, and selectively forming a gate contact on the insulator film, (2) heavily doping the **epitaxial** **layer** with a 1st **cond**.-**type** dopant using the contact as a mask, (3) etching to undercut the exposed side walls of the gate contact and lightly doping the opening with a 1st **cond**.-**type** dopant, (4) diffusing the dopants to form a highly **doped** 1st base **region** on the **epitaxial** **layer** surface and forming a lightly **doped** 2nd base **region** adjacent to the 1st base region, and (5) matching a part of the 1st and 2nd base regions with the gate contact to selectively form a 2nd **cond**.-**type** source region.

L29 ANSWER 15 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:572439 HCAPLUS
DN 115:172439

TI Manufacture of semiconductor devices
IN Saigo, Satoshi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 03034371 | A2 | 19910214 | JP 1989-169489 | 19890629 |
| | JP 2778126 | B2 | 19980723 | | |

AB Manufg. a semiconductor device including both a MOS FET and a Schottky barrier diode involves (1) opening a contact hole in a Si oxide film which is formed on a 1st **cond.-type epitaxial layer** in a Schottky barrier diode region, (2) forming a 2nd **cond.-type doped region** on the area exposed by the opening, (3) carrying out a side-wall deposition on the opening wall, (4) anisotropically etching to remove the exposed 2nd **cond.-type doped region**, (5) forming a silicide layer on the sides and bottom of grooves formed by the etching to provide a Schottky barrier diode. The method allows self-aligned formation of a girdling diffusion layer in the Schottky barrier diode.

L29 ANSWER 16 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:219511 HCAPLUS
DN 114:219511
TI Semiconductor device
IN Watanabe, Tokuo; Sato, Kazue; Nagano, Takahiro; Yadori, Shoji; Nishida, Takashi
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 02271566 | A2 | 19901106 | JP 1989-90719 | 19890412 |
| | JP 2569171 | B2 | 19970108 | | |
| | US 5506156 | A | 19960409 | US 1994-279087 | 19940722 |
| PRAI | JP 1989-90719 | | 19890412 | | |
| | US 1990-508648 | | 19900410 | | |
| | US 1991-814223 | | 19911223 | | |
| | US 1993-37549 | | 19930326 | | |

AB The title device comprises: a 2nd **cond.-type** layer formed epitaxially on a 1st **cond.-type** substrate; a 1st, a heavily-doped 2nd, another 1st and another heavily-doped 2nd **cond.-type** region formed transversely in that order by ion implantation in the upper segment of the substrate; similar but normally-**doped regions** in the **epitaxial layer**; and addnl. components to form monolithically a 1st and a 2nd **cond.-type** channel MOS **transistor** and a high-speed bipolar **transistor**.

L29 ANSWER 17 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:54136 HCAPLUS
DN 114:54136
TI Triple-diffusion-type **transistors**

IN Hara, Tomoki
PA NEC Yamagata, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 02128426 | A2 | 19900516 | JP 1988-283337 | 19881108 |

AB A triple-diffusion-type **transistor** comprises: a 1st-**cond** .-**type** semiconductor substrate; 1st and 2nd buried layers of, resp., the 2nd and 1st **cond**. **types**; a 2nd-**cond** .-**type** lightly-doped **epitaxial layer** on the substrate; 1st and 2nd 1st-**cond**.-**type** collector regions (the 2nd surrounds the 1st) in, resp., the middle and peripheral regions of the **epitaxial layer**, which reach the 2nd buried layer; a 1st-**cond**.-**type** highly-**doped** contact **region** on the 2nd collector region; a 2nd-**cond** .-**type** base region on the **epitaxial layer** surrounded by the 2nd collector region; a 2nd-**cond**.-**type** highly-**doped** base contact **region** sepd. from the 1st collector region; and a 1st-**cond**.-**type** highly-**doped** emitter **region** on the base region contg. the 1st collector region.

L29 ANSWER 18 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:110154 HCAPLUS
DN 112:110154
TI Manufacturing of semiconductor device
IN Oki, Masaru
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 01235368 | A2 | 19890920 | JP 1988-63846 | 19880316 |

AB A method for manufg. a semiconductor device involves the following steps: (1) successively forming a Si nitride film and a 1st Si oxide film on a semiconductor substrate; (2) selectively removing the 1st Si oxide film; (3) implanting impurity ions using the 1st Si oxide film as a mask to form **doped regions** having a 1st **cond**. **type** ; (4) wet etching the 1st Si oxide film to widen its openings; (5) etching the Si nitride film using the 1st Si oxide film as a mask; (6) carrying out selective oxidn. using the Si nitride film as a mask form a 2nd Si oxide film; and (7) implanting impurity ions using the 2nd oxide film as a mask to form **doped regions** having a 2nd **cond** . **type**. Addnl., an **epitaxial film** may be formed on the overall surfaces and often steps may be carried out. The mask mismatching in photolithog. is presented.

L29 ANSWER 19 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:89561 HCAPLUS
DN 112:89561
TI Manufacturing of semiconductor device
IN Hattori, Junichi; Takahata, Koichiro

PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 01194358 | A2 | 19890804 | JP 1988-19420 | 19880128 |

AB The title method involves the following: (1) forming a 1st buried **doped region** having a 1st **cond. type** on a semiconductor substrate; (2) forming a 2nd buried **doped region** having a 2nd **cond. type** next to the 1st region; and (3) forming an **epitaxial layer** on the substrate. By forming the 2nd region, the autodoping in the 3rd step is prevented.

L29 ANSWER 20 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1989:184344 HCAPLUS
DN 110:184344
TI Cascaded-junction field-effect **transistor** manufacture
IN Okano, Junichi; Matsumoto, Kiyohito
PA Toshiba Corp., Japan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 4800172 | A | 19890124 | US 1988-152396 | 19880204 |
| | EP 278410 | B1 | 19930414 | EP 1988-101652 | 19880204 |
| | R: DE, FR, GB | | | | |
| PRAI | JP 1987-26366 | | 19870209 | | |

AB An **epitaxial layer** of a 1st **cond. type**, to serve as the channel region, is grown on a semiconductor substrate of the 2nd **cond. type**, part of the **epitaxial layer** is selectively oxidized to form a thick oxide film, which is removed to provide a part of the surface which is lower than the main surface of the **epitaxial layer**, and the low and high surfaces are doped with an impurity of the 1st **cond. type** to form source and drain regions sepd. by a predetd. distance. The low and high areas between the source and drain **regions** are **doped** with an impurity of the 2nd **cond. type** to form 1st and 2nd junction gates sepd. by a predetd. distance. Then, the substrate is connected to the 2nd junction gate and the source region to connect 2 junction FETs in cascade fashion.

L29 ANSWER 21 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1989:49728 HCAPLUS
DN 110:49728
TI Manufacturing of a semiconductor device by forming an emitter **region** using **doped** polycrystalline silicon films
IN Takemura, Hisashi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese

FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|
| PI JP 63204763 | A2 | 19880824 | JP 1987-38180 | 19870220 |
| JP 06012779 | B4 | 19940216 | | |

AB The title method involves the following steps: (1) successively forming a buried layer having a 2nd **cond.-type** and an **epitaxial layer** on a Si semiconductor substrate having a 1st **cond.-type**; (2) forming a base region having the 1st **cond.-type** in the collector region from the **epitaxial layer**; (3) selectively removing a Si oxide film on the base region to form an opening; (4) forming a polycryst. Si film and doping with an impurity (e.g., As) having the 2nd **cond .-type**; (5) repeating the 4th step to make the polycryst. Si total thickness to .gtoreq.2000 .ANG.; and (6) lamp annealing to effect the impurity diffusion and to form an emitter region. The method is useful for fabricating a **transistor**.

L29 ANSWER 22 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1988:14953 HCAPLUS
DN 108:14953
TI Formation of isolation regions in semiconductor device fabrication
IN Ito, Takao
PA Toshiba Corp., Japan
SO Eur. Pat. Appl., 20 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | EP 236811 | A2 | 19870916 | EP 1987-102343 | 19870219 |
| | EP 236811 | A3 | 19900314 | | |
| | EP 236811 | B1 | 19940413 | | |
| | R: DE, FR, GB | | | | |
| | JP 07105436 | B4 | 19951113 | JP 1986-169245 | 19860718 |
| | US 4810668 | A | 19890307 | US 1987-72446 | 19870713 |
| PRAI | JP 1986-49910 | | 19860307 | | |
| | JP 1986-169245 | | 19860718 | | |
| | EP 1987-102343 | | 19870219 | | |

AB A heavily **doped region** of the 1st **cond. type** for interdevice isolation and a heavily **doped region** of the 2nd **cond. type** in the device region are formed on the surface of a substrate of the 1st **cond. type**, and an **epitaxial layer** is grown on the substrate, forming buried regions by expansion of the heavily **doped regions**. A 1st groove is formed which reaches the heavily **doped region** of the 1st **cond. type** for interdevice isolation, and a 2nd groove is formed which reaches the buried region of the 2nd **cond. type** for intradevice isolation of a vertical bipolar **transistor**, and substantially insulative isolation material is buried in the grooves.

L29 ANSWER 23 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1986:636914 HCAPLUS
DN 105:236914
TI Isolation of bipolar **transistors**
IN Fukuda, Takeshi; Akatsuka, Tsutomu
PA Fujitsu Ltd., Japan

SO Jpn. Tokkyo Koho, 3 pp.
CODEN: JAXXAD
DT Patent
LA Japanese
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | JP 61029539 | B4 | 19860707 | JP 1979-61233 | 19790518 |
| | JP 55153344 | A2 | 19801129 | | |

AB A method for forming a semiconductor device (e.g., a bipolar **transistor**) includes: (a) forming an oxide film (e.g., SiO2) on an **epitaxial layer** formed on a substrate; (b) forming a thin film (e.g., Si3N4) on the oxide film with openings, (c) implanting an impurity (e.g., B) having the same **cond**. **type** as the base region into the surface of the **epitaxial layer** with the thin film as a mask; (d) diffusing the impurity by annealing at .apprx.1000.degree.; (e) forming V-shaped device isolation regions with an insulator (e.g., polycryst. Si) in the **doped regions**; (f) forming a photoresist film which exposes the intended base region; (g) removing the thin film and the oxide film with the resist as a mask; (h) forming the base region between the device isolation regions; and (i) forming the emitter region on the base region with the device isolation regions as a mask. The method can easily form bipolar **transistors** with insulator filled V-shaped device isolation regions.

L29 ANSWER 24 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1980:629749 HCAPLUS
DN 93:229749
TI Semiconductor device
IN Oikawa, Saburo; Murakami, Susumu; Terasawa, Yoshio
PA Hitachi, Ltd., Japan
SO Ger. Offen., 20 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | DE 3012119 | A1 | 19801002 | DE 1980-3012119 | 19800328 |
| | DE 3012119 | C2 | 19851107 | | |
| | US 4329772 | A | 19820518 | US 1980-134673 | 19800327 |
| | FR 2452784 | A1 | 19801024 | FR 1980-7106 | 19800328 |
| | FR 2452784 | B1 | 19850308 | | |
| PRAI | JP 1979-37034 | | 19790330 | | |

AB In the fabrication of a FET, a field-controlled thyristor, or an **integrated circuit**, autodoping is eliminated by forming a mask on a semiconductor substrate, doping the substrate through openings in the mask to form regions of the opposite **cond**. **type** , removing the mask and forming another with smaller openings so that the mask extends beyond the edges of the **doped regions**, growing **epitaxial layers** in the openings in the 2nd mask, and heat treating to expand the **doped regions** until the channels between them are narrower than the **epitaxial layers**.

L29 ANSWER 25 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1980:139655 HCAPLUS
DN 92:139655
TI **Integrated circuits**

IN Richer, John Wilfred
PA International Computers Ltd., UK
SO S. African, 21 pp.
CODEN: SFXXAB
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | ZA 7805953 | A | 19790926 | ZA 1978-5953 | 19781023 |
| | AU 7841285 | A1 | 19790517 | AU 1978-41285 | 19781102 |
| | FR 2408217 | A1 | 19790601 | FR 1978-31208 | 19781103 |
| PRAI | GB 1977-45719 | | 19771103 | | |

AB A method is described for forming **integrated circuits** with buried **transistors** having improved high-speed performance. The method consists of forming a 1st buried region of a predetd. **cond. type** by diffusion of a dopant into a substrate of opposite **cond. type**, subsequently depositing an **epitaxial layer** of the 2nd **cond. type** on the substrate surface to bury the 1st region, and forming shallow circuit elements consisting of zones of predetd. different **cond. types** at the exposed surface of the **epitaxial layer** overlying the buried 1st region. The improvement consists of forming, subsequent to the formation of the 1st region, a 2nd region of 1st **cond. type** within the area of the substrate in which the 1st region is located, and subsequently growing the 2nd region by diffusion to a predetd. penetration depth into the area of the **epitaxial layer** overlying the 1st region to convert at least part of the **epitaxial layer** adjacent to the 1st region to 1st **cond. type** in the area overlying the 1st region. For example, a p-type Si slice with an oxide mask is doped with slow-diffusing As to form a n-type region below the windows of the mask. A layer of carefully controlled thickness contg. fast-diffusing P dopant is then formed over the mask, and this assembly is then subjected to a high-temp. diffusion operation during which the P diffuses to a predetd. depth into the n-type layer in the regions of the windows, but is prevented from further diffusion into the slice by the remainder of the mask. The oxide layer is then removed and a p-type **epitaxial layer** is deposited over the slice to bury the P-**doped region**. Further diffusion operations are then carried out to form **transistors** with a higher gain band width.

L29 ANSWER 26 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1975:601123 HCAPLUS
DN 83:201123
TI Guarded planar PN junction semiconductor device
IN Wolley, Elden D.
PA Westinghouse Electric Corp., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 3909119 | A | 19750930 | US 1974-440203 | 19740206 |
| | JP 50110780 | A2 | 19750901 | JP 1975-14936 | 19750206 |
| PRAI | US 1974-440203 | | 19740206 | | |

AB A guarded planar p-n junction device with moderate breakdown voltages is

described, which can be fabricated easily with std. photolithog. techniques. The device avalanches uniformly at the interior of the junction, avoiding thermal failure. First and 2nd impurity regions of opposite **cond**. **type** are positioned in the semiconductor body, which may be a single crystal **wafer**, or an **epitaxial layer** on a degenerate conductive semiconductor substrate. The 2nd impurity region has a sufficiently low impurity concn. profile and a sufficiently large thickness to support a space-charge region formed at the junction on application of a given reverse bias voltage across the junction. A 3rd impurity region of opposite **cond**. **type** from the 1st and of the same **cond**. **type** as the 2nd impurity region adjoins the major surface contiguously around the 1st impurity region and at least laterally contiguously around the 1st and 2nd impurity regions in the interior of the body, forming a 2nd p-n junction contiguously around the 1st junction. The 3rd impurity region has an impurity concn. profile and thickness such that the space-charge region formed at the 2nd junction is greater than that formed at the 1st under reverse bias. The blocking voltage can thereby be controlled by the avalance breakdown or punch-through voltage at the 2nd impurity region. The resistivity of the uniformly **doped** 3rd impurity **region** is .gtoreq.2 times greater than the av. resistivity of the 2nd impurity region. Devices with a 4th impurity region are also described. The devices can be provided with insulated electrode layers which axially extend the space charge region of the 2nd junction at the major surface. **Transistors** and thyristors employing these junctions are illustrated.

L29 ANSWER 27 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1972:51789 HCAPLUS
DN 76:51789
TI Depletion layer capacitor in particular for monolithic **integrated circuits**
IN Schilling, Harald
PA International Telephone and Telegraph Corp.
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | US 3584266 | A | 19710608 | US 1969-826146 | 19690520 |
| | DE 1764398 | A | 19710204 | DE 1967-1764398 | 19680530 |
| | DE 1764556 | A | 19700910 | DE 1967-1764556 | 19680626 |
| | DE 1764556 | C3 | 19790104 | | |
| | GB 1239377 | A | 19710714 | GB 1969-1239377 | 19690521 |
| | FR 2009973 | B1 | 19730525 | FR 1969-17511 | 19690529 |
| | BE 733819 | A | 19691201 | BE 1969-733819 | 19690530 |
| | NL 6908238 | A | 19691202 | NL 1969-8238 | 19690530 |
| | US 3581164 | A | 19710525 | US 1969-834428 | 19690618 |
| | BE 735089 | A | 19691229 | BE 1969-735089 | 19690625 |
| | FR 2014235 | A5 | 19700417 | FR 1969-21310 | 19690625 |
| | NL 6909793 | A | 19691230 | NL 1969-9793 | 19690626 |
| PRAI | DE 1967-1764398 | | 19680530 | | |
| | DE 1967-1764556 | | 19680626 | | |

AB A depletion-layer capacitor was manufd. which has a relatively high breakdown voltage and a high specific capacitance. The capacitor can be formed simulaneously with planar **transistors** on a monolithic **integrated circuit**. The capacitor achieves a high

voltage breakdown by producing a p-n junction which joins 2 highly **doped regions** of opposite **cond. type** , wherein the junction is established within an **epitaxial layer** of lower impurity concn. and does not extend to the surface of the **epitaxial layer**. The capacitor comprises a **wafer** of a material of a given **cond. type**; a 1st region of the opposite **cond. type**; a 2nd region of the given **cond. type**; and means around the 1st and 2nd regions for effectively maintaining a p-n junction.

L29 ANSWER 28 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1972:39083 HCAPLUS
DN 76:39083
TI Semiconductor device
IN Augusta, Benjamin
PA International Business Machines Corp.
SO Brit., 6 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | GB 1251768 | | 19711027 | | |
| PRAI | US | | 19690630 | | |

AB A semiconductor device was manufd. which comprises a substrate having a 1st semiconductor region of a 1st **cond. type**, an **epitaxial layer** of semiconductor material of opposite **cond. type**, a diffused 2nd semiconductor region of the 1st **cond. type** defining an isolation wall extending from the 1st region through the layer to the surface and circumscribing internally a portion of the layer, defining a pocket region for a resistor element, and a diffused 3rd semiconductor region of the opposite **cond. type** defining the resistor element formed within the pocket region, spaced from the 1st and 2nd regions, and having a resistivity substantially less than the resistivity of the remaining portion of the pocket region. In a preferred example, the substrate is single-crystal Si having a region of p-type cond., and it has a planar surface over which an n-type layer is grown epitaxially. The dopant for the p-type region is B, and the dopant for the n-type **epitaxial layer** is P or As. The isolation region, of p-type cond., is diffused through the n-type **epitaxial layer**. The resistor region is formed as a discrete highly **doped** n+ **region** by diffusion of P or As.

L29 ANSWER 29 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1971:524343 HCAPLUS
DN 75:124343
TI Semiconductor **integrated circuit** with reduced minority carrier storage effect
IN Makimoto, Tsugio
PA Hitachi, Ltd.
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

| PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
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| PI US 3596149 | A | 19710727 | US 1970-4468 | 19700119 |
| US 3735481 | A | 19730529 | US 1971-118615 | 19710225 |
| PRAI JP 1967-52220 | | 19670816 | | |
| US 1968-752049 | | 19680812 | | |
| US 1970-4468 | | 19700119 | | |

AB A semiconductor **integrated circuit** is provided, consisting of diodes and (or) **transistors** with a reduced minority carrier voltage effect and switching elements with a suitably increased one, thus improving the switching characteristic. A 1st-**cond**.-**type** layer having a relatively low surface impurity concn. is epitaxially grown on the surface of a 1st **cond** . **type** substrate having a no. of 2nd-**cond**.-**type** buried layers in one major surface. The layer is divided into a no. of elec. isolated portions by 2nd-**cond**.-**type** regions, which are formed by diffusing a 2nd-**cond**.-**type** -detg. impurity in a closed ring shape into the surface of the layer toward the buried layers. The divided portions constitute individual switching elements, e.g. diodes and **transistors**, the buried layers and the 2nd-**cond**.-**type** impurity regions serving as their structural elements. In forming the **transistors**, the 1st-**cond**.-**type** highly **doped region** is selectively formed in one portion of the **epitaxial layer**, surrounded with the buried layers and the 2nd-**cond** .-**type** regions. Second-**cond**.-**type** highly **doped regions** are selectively formed as the emitter regions in the 1st highly **doped region**. The buried layers and the 2nd-**cond**.-**type** regions connected to them are used as collector regions. The 1st-**cond**.-**type** highly **doped regions** and the **epitaxial layers** having a low surface impurity concn. serve as the base regions with a gradient of impurity concn. The width of the base regions is less than the diffusion length of the minority carrier existing in them. Diodes having highspeed recovery are obtained simultaneously by fitting one electrode to the emitter regions of different **transistors** formed in the 2nd isolated regions and the other electrode to their base-collector junctions. In forming the diodes, 2nd-**cond**.-**type** highly **doped regions** are formed in the 3rd isolated regions simultaneously with the formation of the emitter regions of the **transistors** to constitute still other **transistors** not having the 1st-**cond**.-**type** highly **doped regions**. A pair of electrodes is fitted to the collector regions and the emitter-base junctions of the individual **transistors** obtained. The 4th isolated region is used as a resistor by forming a pair of electrodes in 2 different portions.

L29 ANSWER 30 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1969:486085 HCAPLUS
DN 71:86085
TI Semiconductor device
PA Radio Corp. of America
SO Brit., 7 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | GB 1161354 | | 19690813 | | |
| PRAI | US | | 19660908 | | |

AB An improved single-crystal semiconductor body is provided with adjacent regions of different cond. characteristics, wherein the impurity concn. of each region has greater uniformity that can be provided by diffusion techniques. This is accomplished by growing a 1st **epitaxial layer** of semiconductor material having a given cond. characteristic onto a substrate, then removing spaced portions of this layer to expose the substrate. Next, a 2nd **epitaxial layer** of semiconductor material is grown over the remaining portions of the 1st layer and the exposed portions of the substrate. The 2nd layer of semiconductor material has a cond. characteristic different from that of the 1st layer . Surface portions of the 2nd layer are then removed to expose the remaining portions of the 1st layer. The resulting structure is a substrate having a no. of adjacent regions of different cond. characteristic semiconductor material suitable for **integrated-circuit** device fabrication. It provides a continuous thin structure of single-crystal semiconductor material having contiguous regions of different cond. characteristics, each of which may have a substantially uniform concn. of doping impurity or impurities. Since the **regions** are uniformly **doped** in a controlled manner, they are esp. suitable for having devices such as bipolar **transistors** fabricated therein. And since there may be adjacent regions of opposite **cond. types**, both p-n-p and n-p-n **transistors** can be fabricated side-by-side with a min. of sep. operations.

L29 ANSWER 31 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1967:41767 HCAPLUS
DN 66:41767
TI Reverse epitaxial **transistor**
PA Fairchild Camera and Instrument Corp.
SO Brit., 11 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

| | PATENT NO. | KIND | DATE | APPLICATION NO. | DATE |
|---|---|---|---|---|---|
| PI | GB 1050478 | | 19661207 | | |
| PRAI | US | | 19621008 | | |

AB In this **transistor** configuration, the usual order of the regions is reversed. The emitter region lies most deeply within the **wafer** . The base region lies above the emitter region. The collector region lies between the base region and the surface. The emitter can be connected together and grounded through the bulk material of the **wafer**. This internal connection eliminates the need for any external connection between the emitters. The collector junctions can be made shallower with less inherent capacitance shunting them to improve high-frequency performance. The shallower collector region minimizes the collector charge storage when the **transistor** is operated in a satn. condition. Five methods for manufg. these **transistors** are given. In the 1st method, an impurity is diffused into the **wafer** to form a heavily **doped** emitter **zone** of the same **cond. type** as the substrate and which is disposed partly within the substrate and partly within the **epitaxial layer**. An impurity is diffused into the **epitaxial layer** to establish a base extending from the surface of the **epitaxial layer** to the emitter zone with an opposite cond. from the emitter. An impurity is then diffused into the base zone at the surface of the **epitaxial layer** to form a

collector zone. In the 2nd method, an impurity is diffused through a limited area of **epitaxial layer** from an exterior surface of the layer to form an emitter zone. The **epitaxial layer** is outdiffused from the exterior surface to leave the emitter buried within the **wafer**. In the 3rd method, an impurity is diffused into a limited area of the exterior surface of the **epitaxial layer** to form an emitter zone. An addnl. **epitaxial layer** is deposited on the exterior surface to bury the emitter zone within the **wafer**. In the 4th method, a very high concn. of impurity is diffused into a limited area of the surface of the heavily doped substrate to form an emitter. An **epitaxial layer** which is lightly doped is deposited on the substrate surface and has the same **cond. type** as the substrate to bury the emitter zone. In the 5th method, 2 heavily **doped zones** are diffused into a surface of a substrate of the same **cond. type**. One zone surrounds the other on the surface and the dopant has a more rapid diffusion rate than that of the zone. A lightly doped **epitaxial layer** is deposited on the substrate surface and diffused into the surrounding zone through the **epitaxial layer** to form a buried emitter beneath the base extending to the exposed surface of the **epitaxial layer**. For example, in an epitaxial **transistor** the concn. of anti-impurities in the emitter region beneath the emitter-base junction was .apprx.9 .times. 1020 atoms P/cc. B was used as the p-type impurity to form a base at a concn. of .apprx.1019 atoms/cc. When current was passed from the emitter to the collector to achieve a collector current of .apprx.5 ma., the device had a forward current gain of .apprx.35; the reverse current gain was .apprx.30.